

The diagram illustrates a card management system 100, which is divided into two main functional blocks: 104 (left) and 111 (right).

Block 104: This block contains a CPU 101, RAM 102, and a Slot 103. The CPU 101 is connected to the RAM 102, which is in turn connected to the Slot 103.

Block 111: This block contains a Host I/F 112, CPU 113, RAM 114, ROM 115, Memory controller 116, First memory 118, Second memory 119, and a database 117. The Host I/F 112 is connected to the CPU 113, which is connected to the RAM 114 and ROM 115. The CPU 113 is also connected to the Memory controller 116. The Memory controller 116 is connected to the First memory 118 and the Second memory 119. The First memory 118 contains Card info. storage 132. The Second memory 119 contains Host info. storage 133. The database 117 contains Address management information 130 and User data 131.

Internal Connections in Block 104: The CPU 101 is connected to the RAM 102, which is connected to the Slot 103. The Slot 103 is connected to the Host I/F 112 in block 111.

Internal Connections in Block 111: The Host I/F 112 is connected to the CPU 113. The CPU 113 is connected to the RAM 114 and ROM 115. The CPU 113 is also connected to the Memory controller 116. The Memory controller 116 is connected to the First memory 118 and the Second memory 119. The First memory 118 contains Card info. storage 132. The Second memory 119 contains Host info. storage 133. The database 117 is connected to the Memory controller 116. The database 117 contains Address management information 130 and User data 131.

Internal Connections in Block 105: The Application program 105 is connected to the File system controller 106. The File system controller 106 is connected to the Access condition determination 107. The Access condition determination 107 is connected to the Card info. acquisition 108. The Card info. acquisition 108 is connected to the Access controller 109. The Access controller 109 is connected to the Condition storage 110. The Condition storage 110 is connected to the File system controller 106.

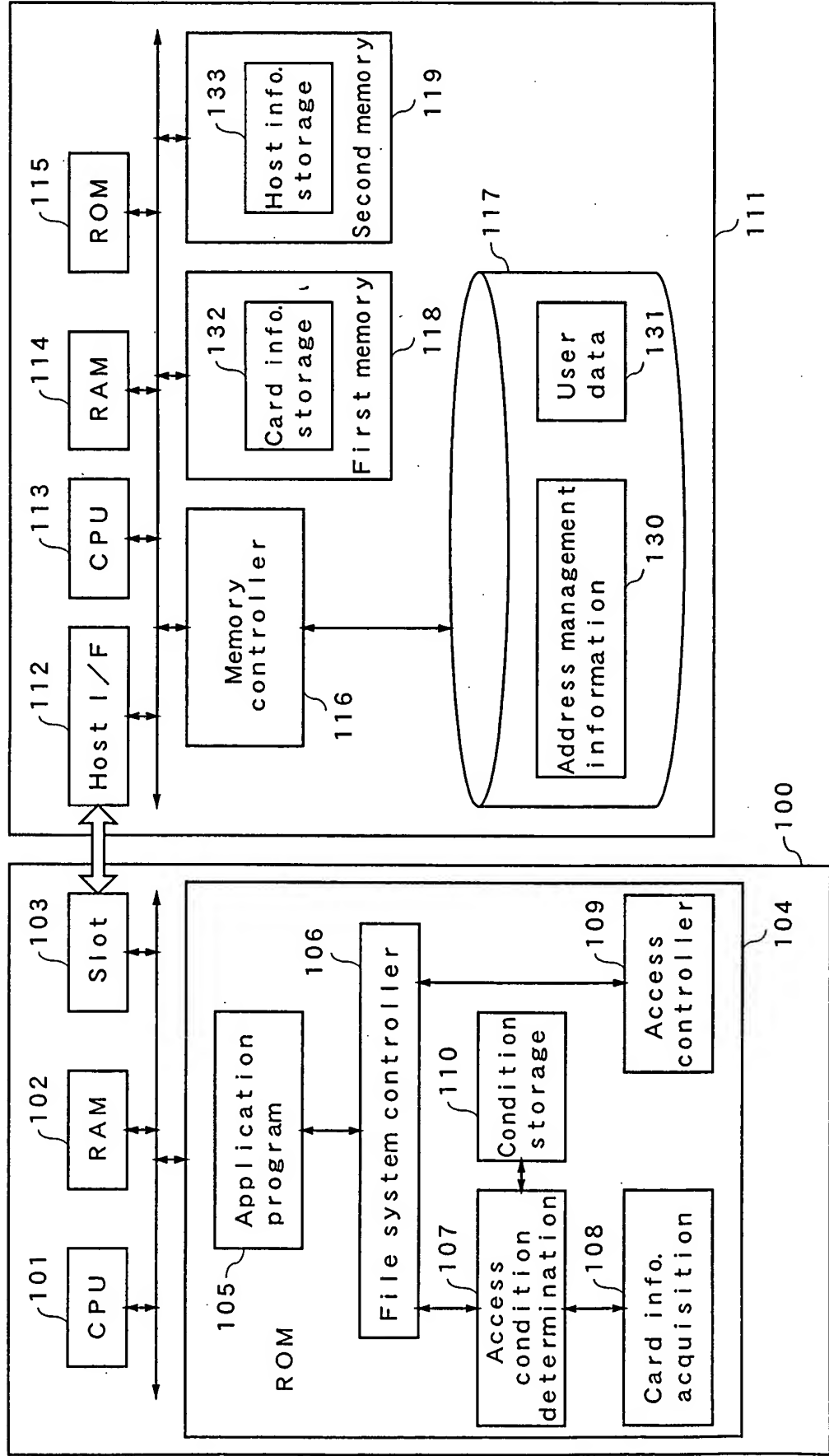


FIG. 2

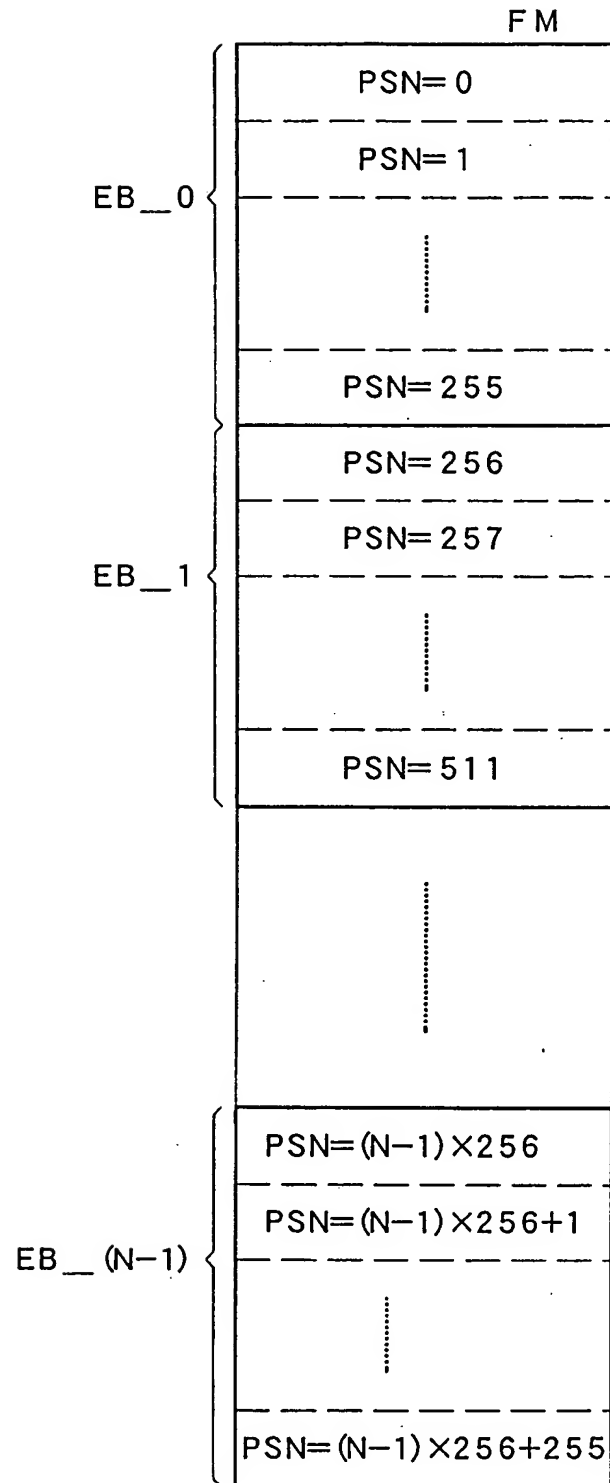


FIG. 3

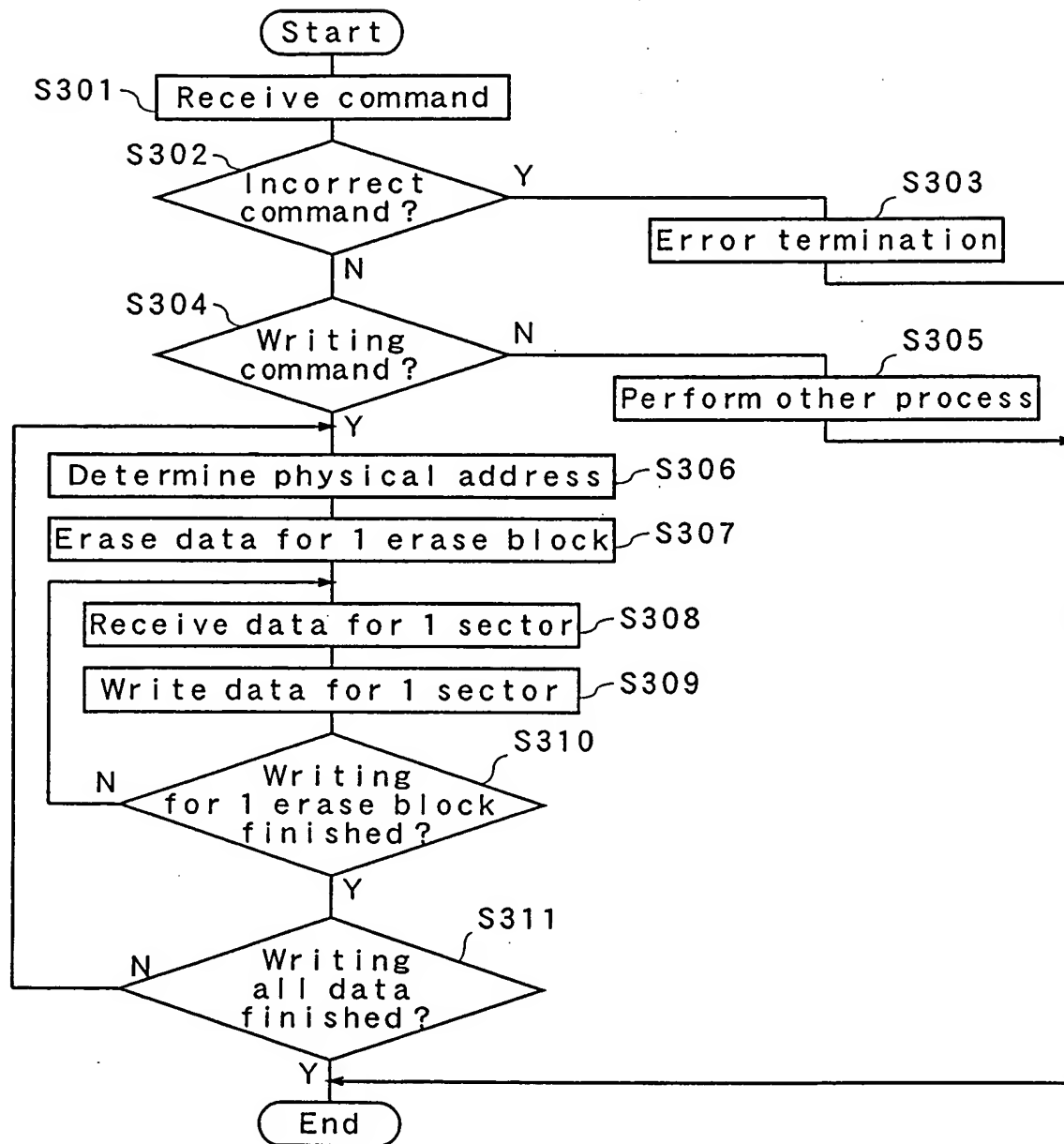


FIG. 4

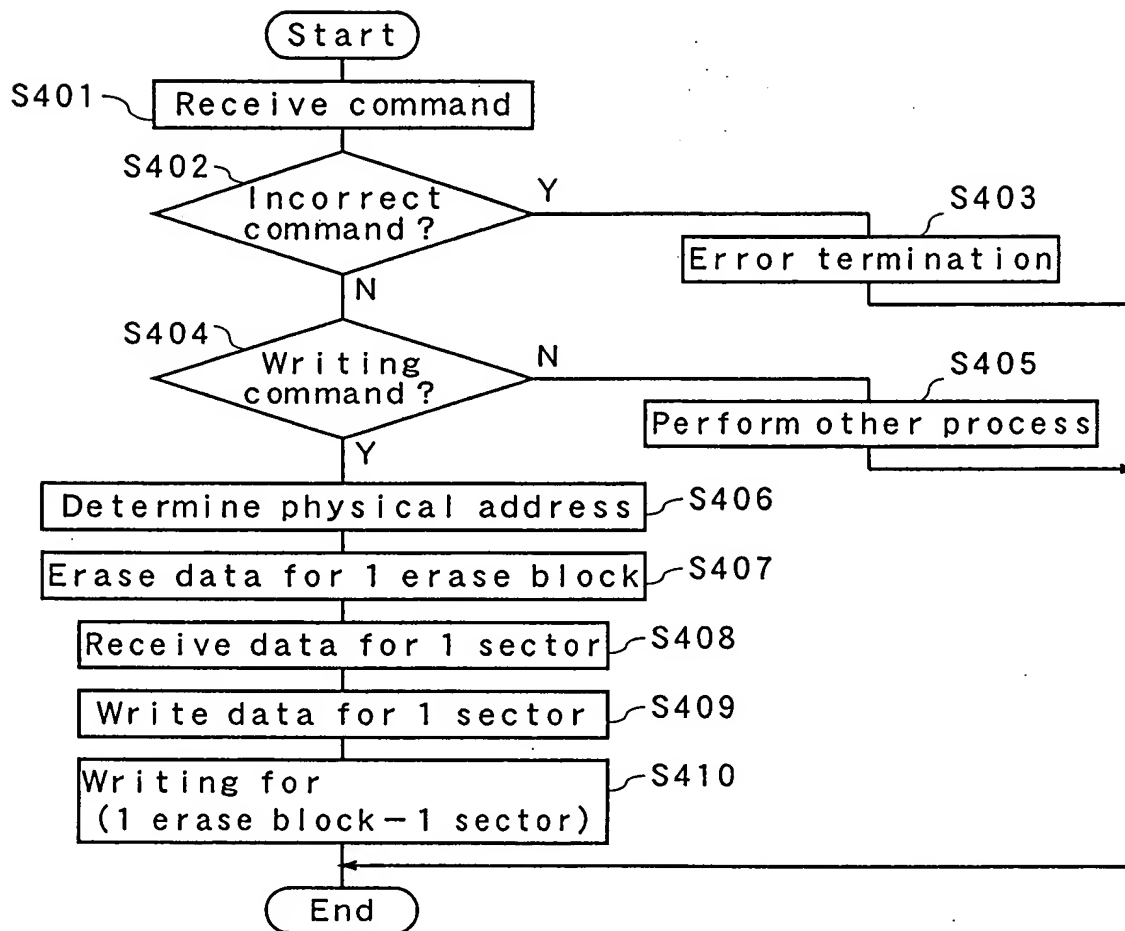


FIG. 5

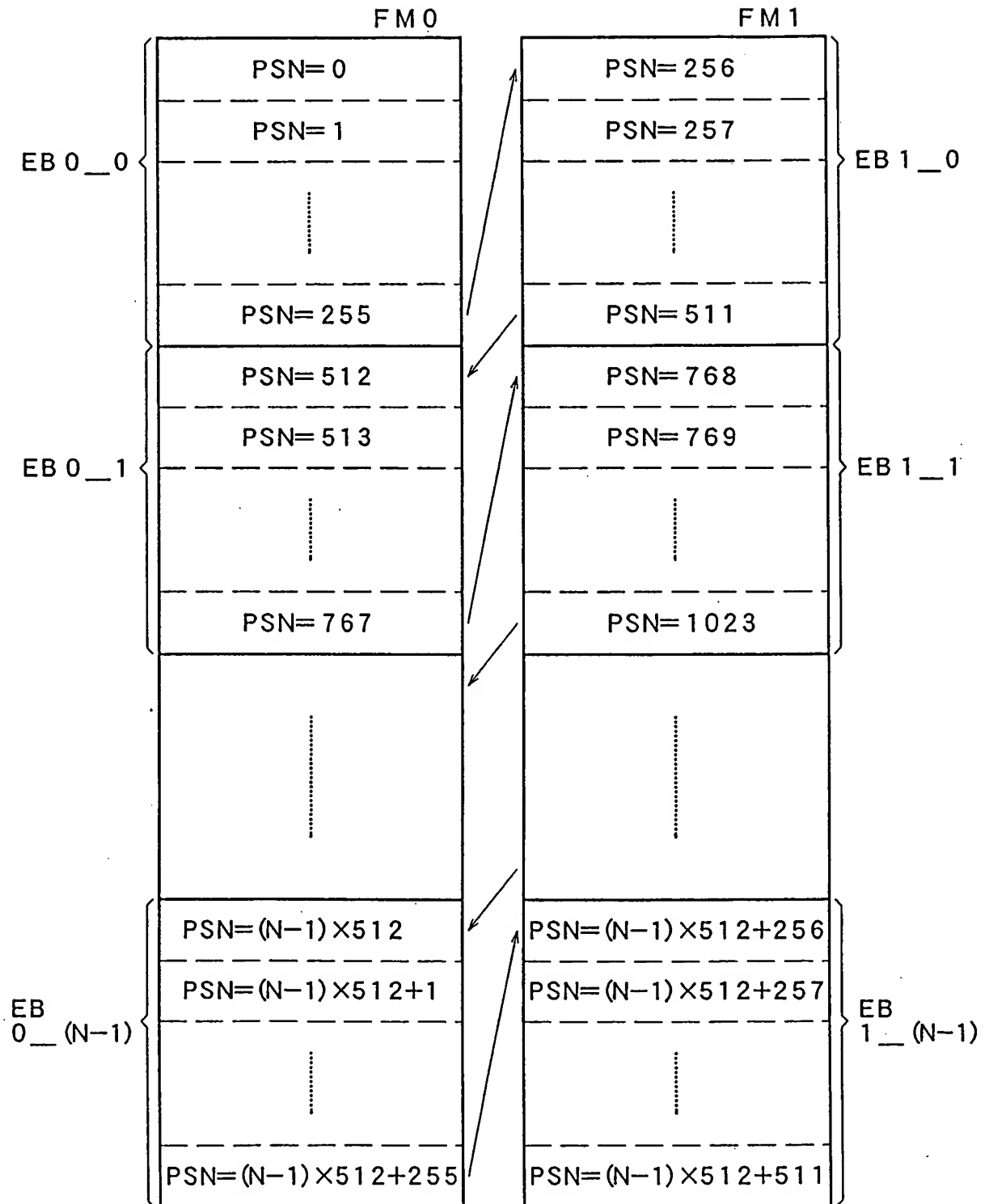


FIG. 6

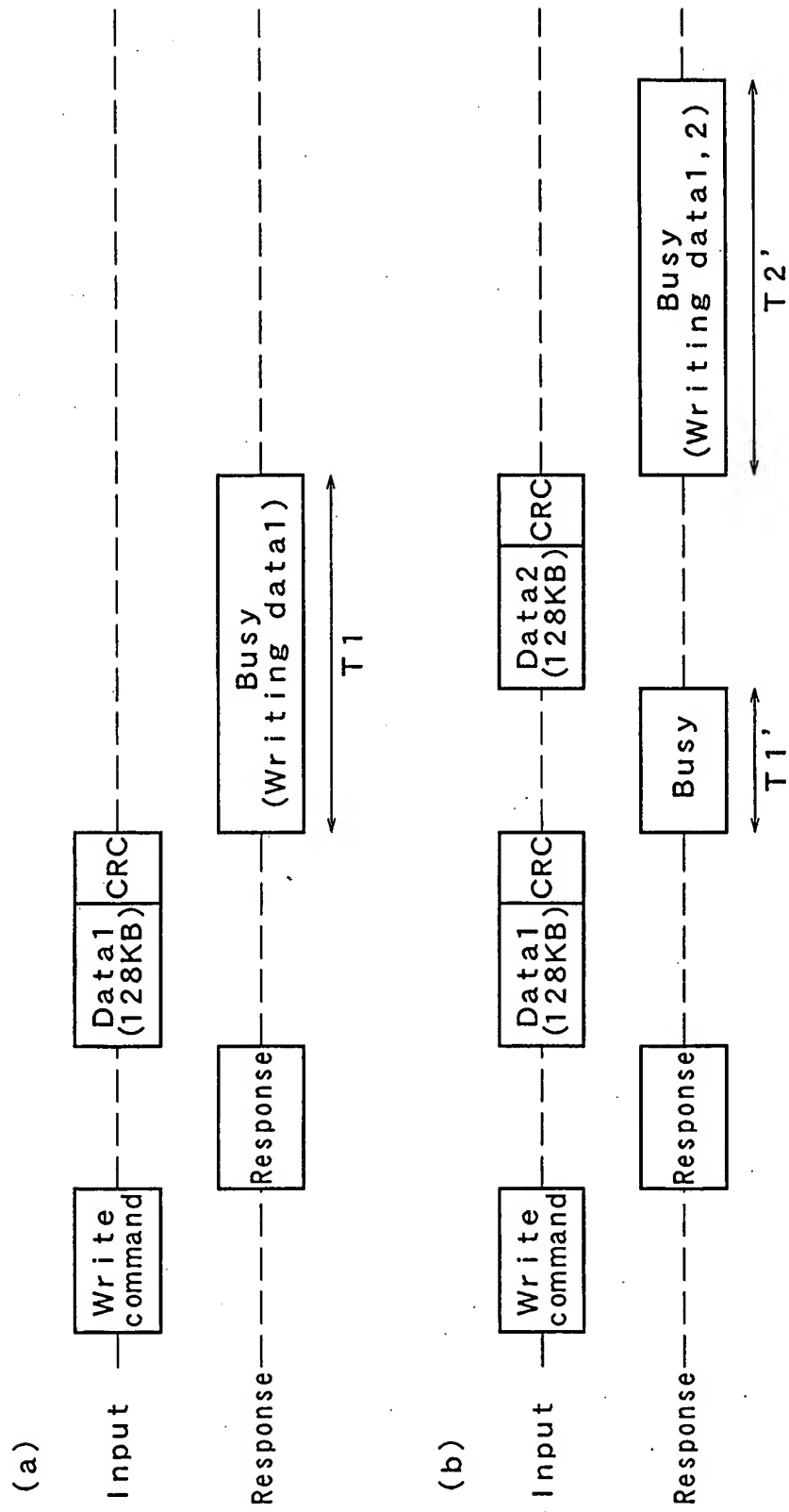


FIG. 7

Types	Items
First info.	Memory type
	The number of memories
	Management method of memory
	Erase block size
	Management block size
	Temperature condition
	Power consumption
	Current value
	Voltage value
	Card type
Second info.	Process type
	Process unit size
	Process unit boundary
	Process unit time
	Access method
	Min. sequential area at S.A
	Input clock frequency
	Bit width
Third info.	Rate performance level
	Data size/Unit time
	Process time/Unit size
	Transfer rate
	Process time inside card
Fourth info.	Error occurrence probability
	Worst value of error notification time
Fifth info.	Rate performance level determination ref.
	Rate performance level
	Power consumption level

FIG. 8

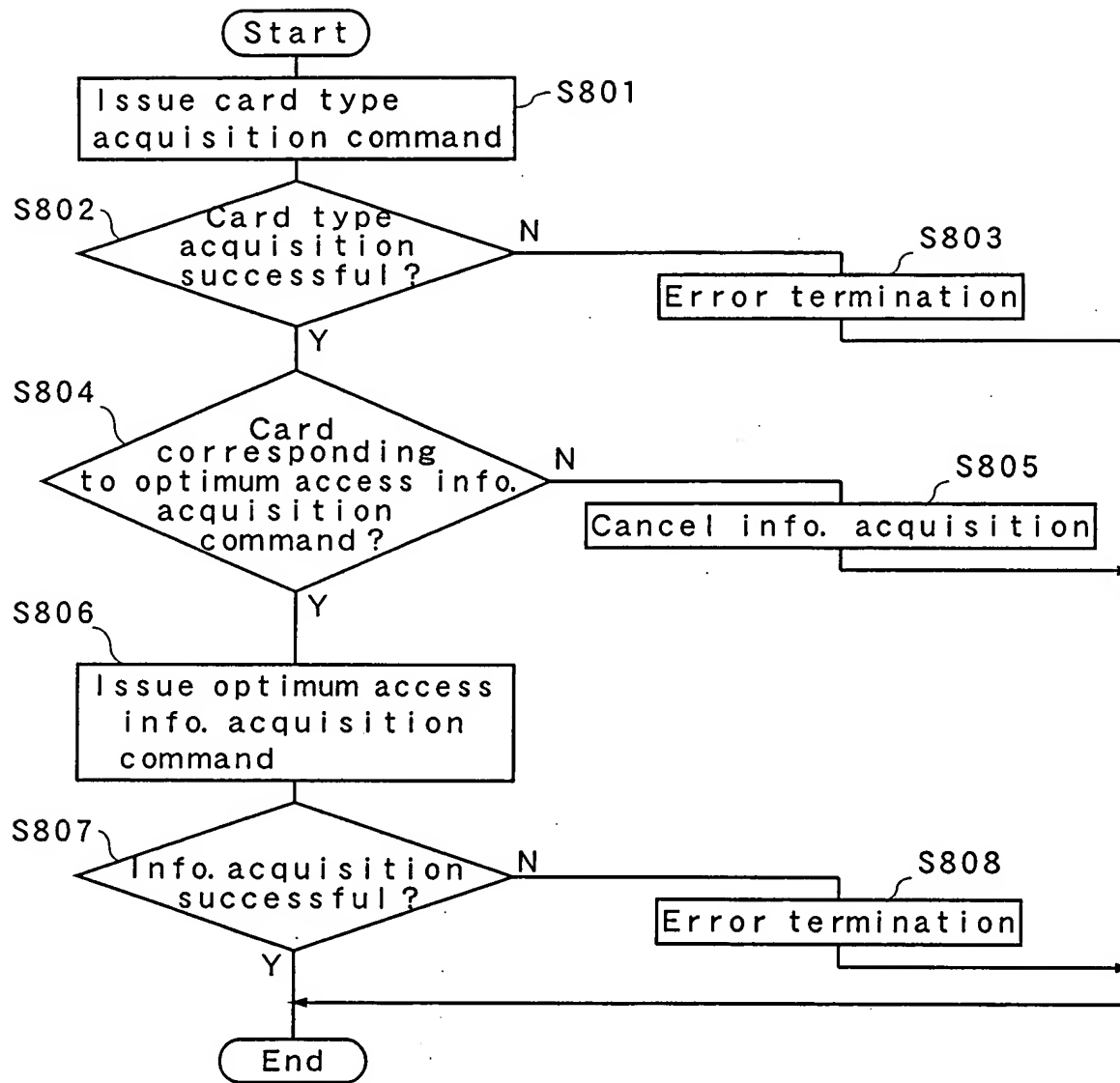


FIG. 9

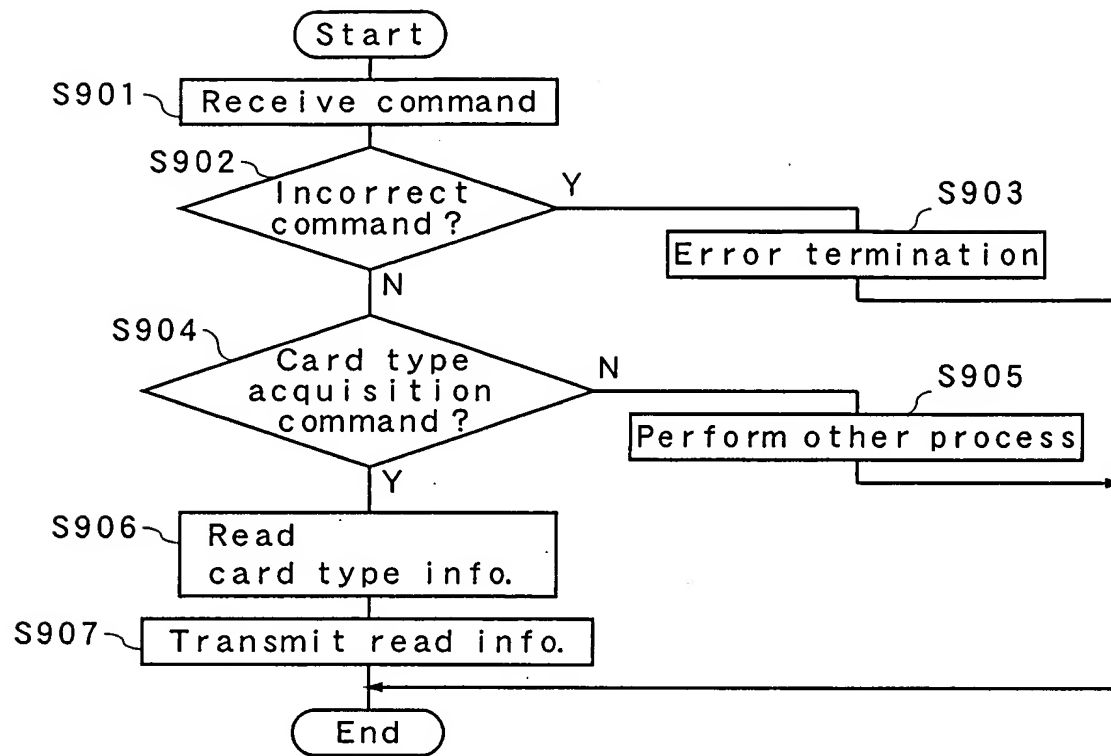


FIG. 10

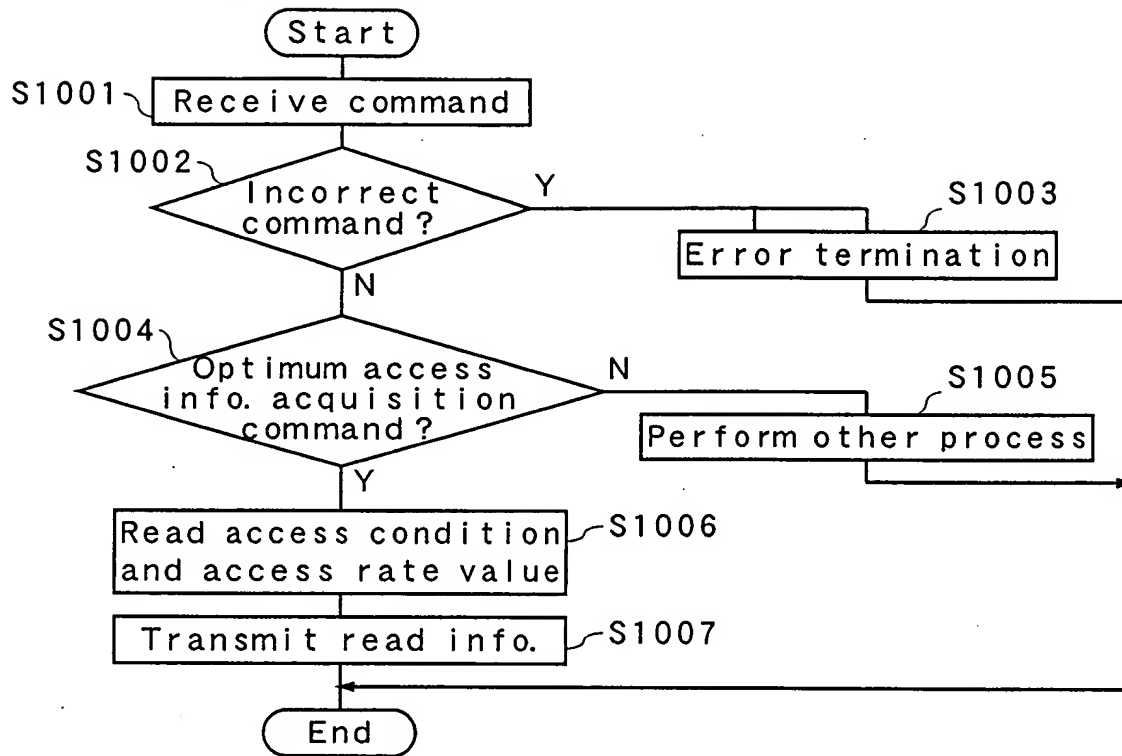


FIG. 11

(a)

Items	Condition values
Process unit size	Multiple length of 128KB
Process unit boundary	Multiple length of 128KB
Access method	Sequentially accessing to sequential area having 256KB over
Input clock frequency	25MHz over
Bit width	4 bits

(b)

Transfer rate of reading(standard) = 11 MB/s
Transfer rate of writing(standard) = 10 MB/s
Transfer rate of erasing(standard) = 10.3 MB/s
Transfer rate of reading(worst) = 6 MB/s
Transfer rate of writing(worst) = 5 MB/s
Transfer rate of erasing(worst) = 5.1 MB/s

FIG. 12

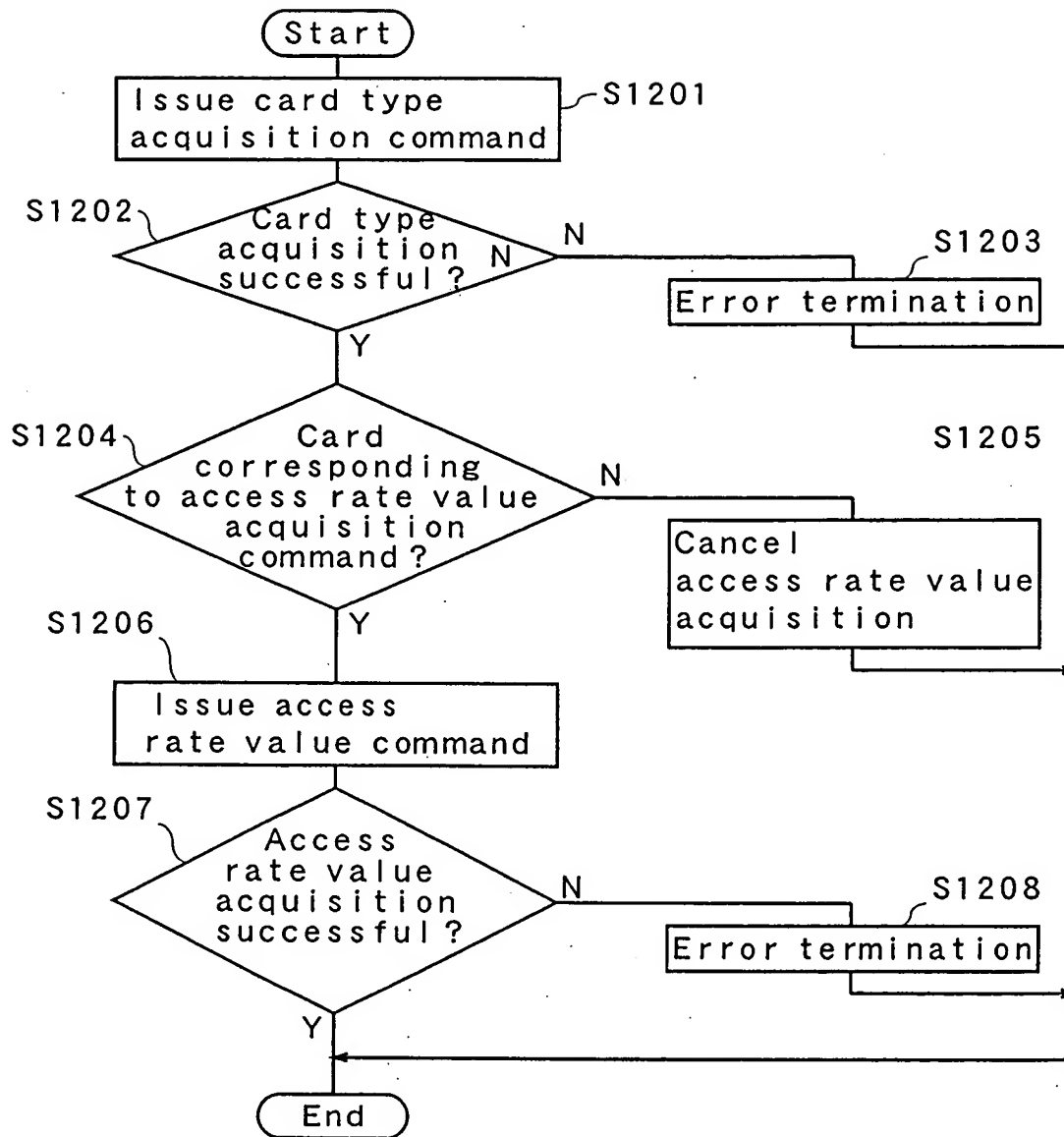


FIG. 13

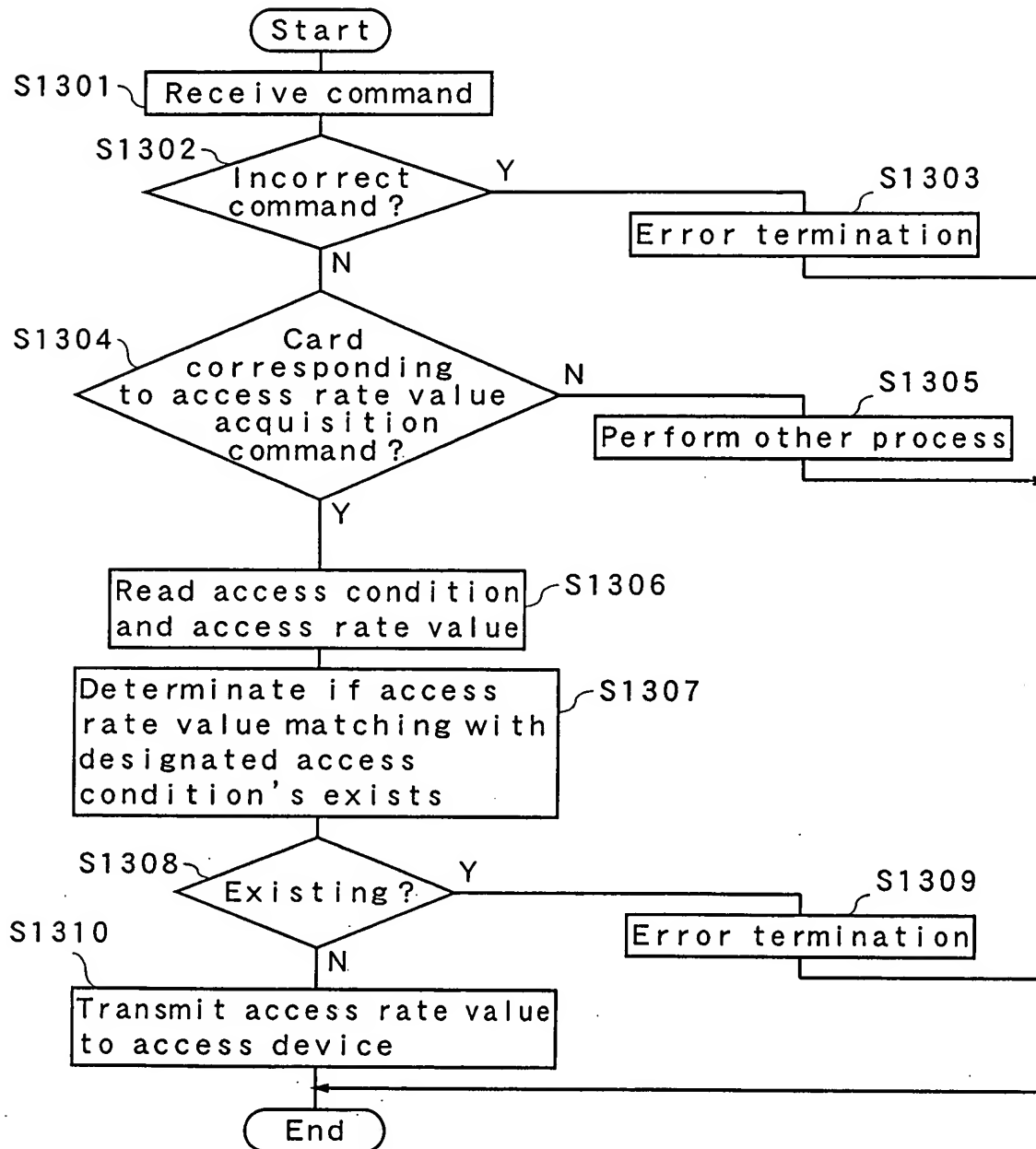


FIG. 14

(a)

Items	Condition values
Process unit size	128 KB
Process unit boundary	128 KB
Access method	Sequentially accessing to sequential area having 256 KB
Input clock frequency	25 MHz
Bit width	4 bits

(b)

Transfer rate of reading(standard) = 11 MB/s
Transfer rate of writing(standard) = 10 MB/s
Transfer rate of erasing(standard) = 10.3 MB/s
Transfer rate of reading(worst) = 6 MB/s
Transfer rate of writing(worst) = 5 MB/s
Transfer rate of erasing(worst) = 5.1 MB/s

FIG. 15

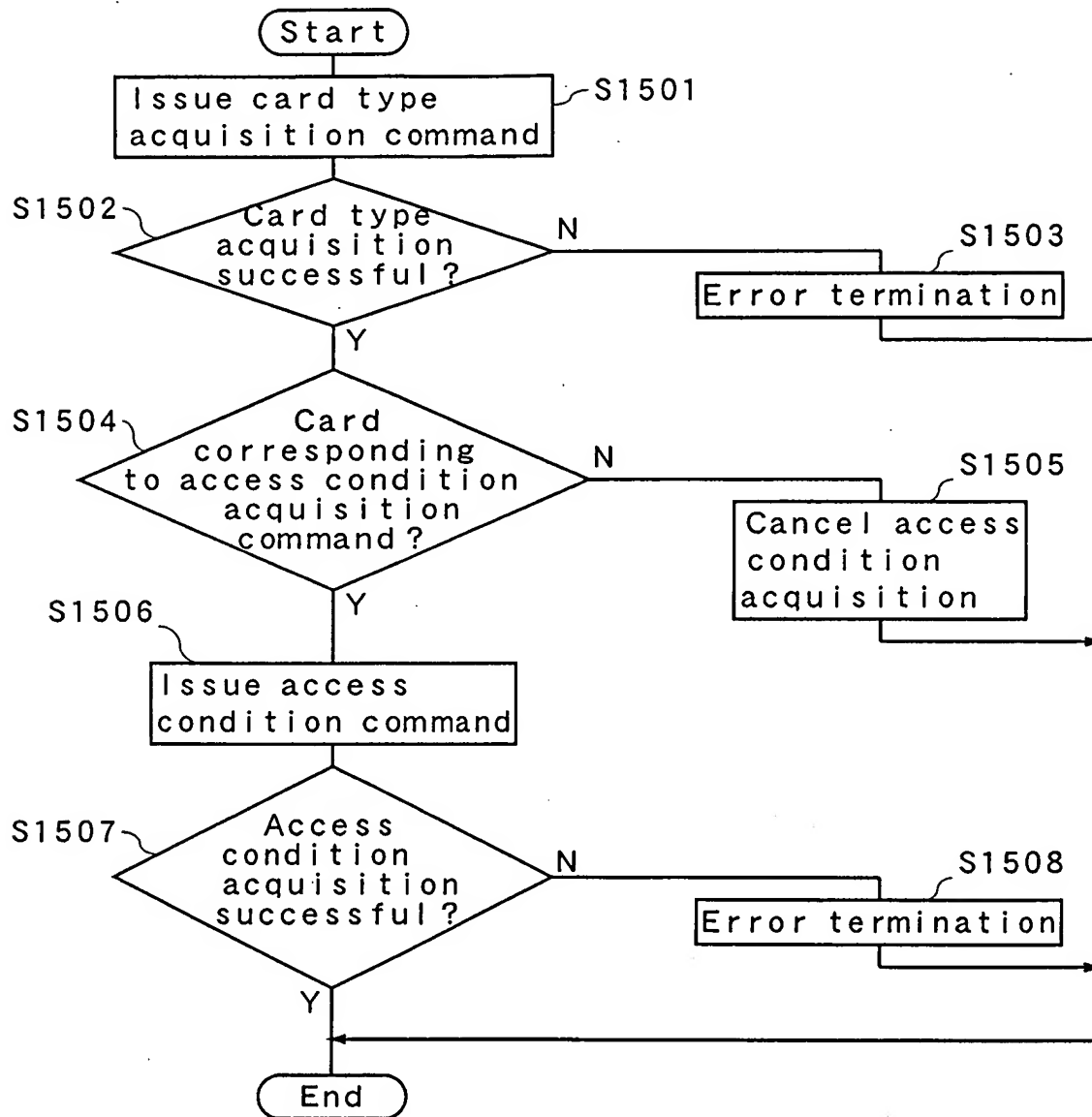


FIG. 16

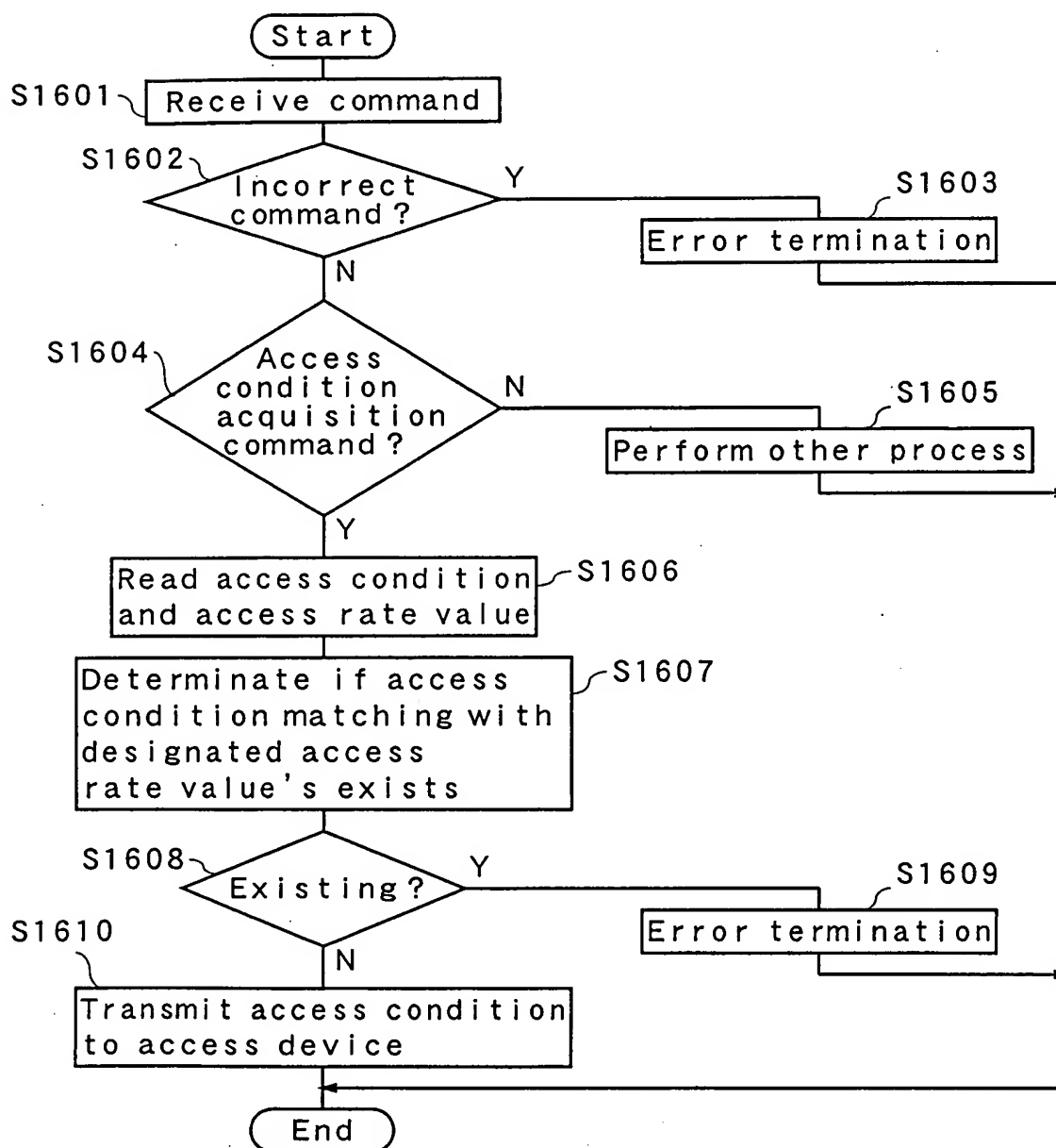


FIG. 17

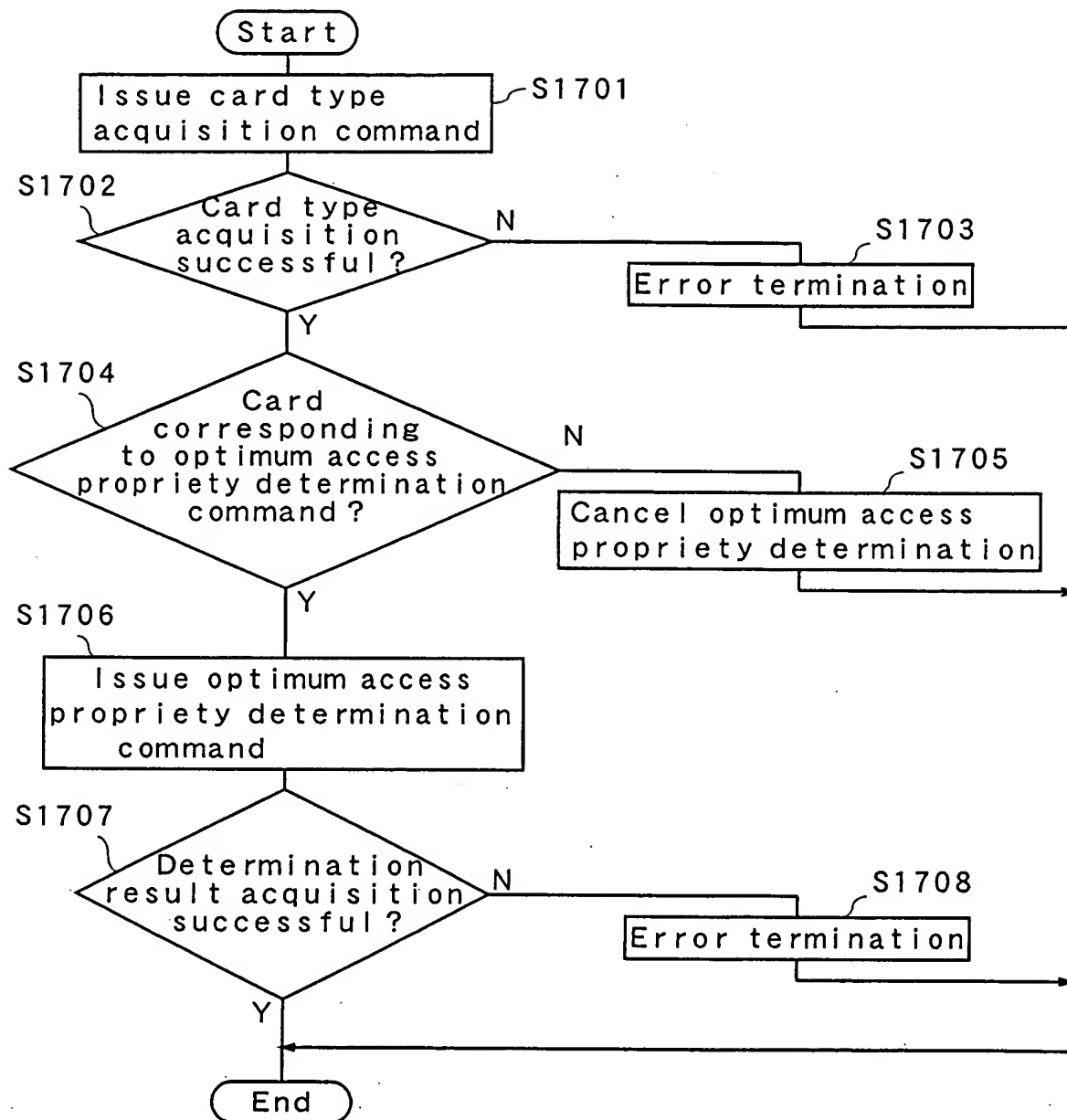


FIG. 18

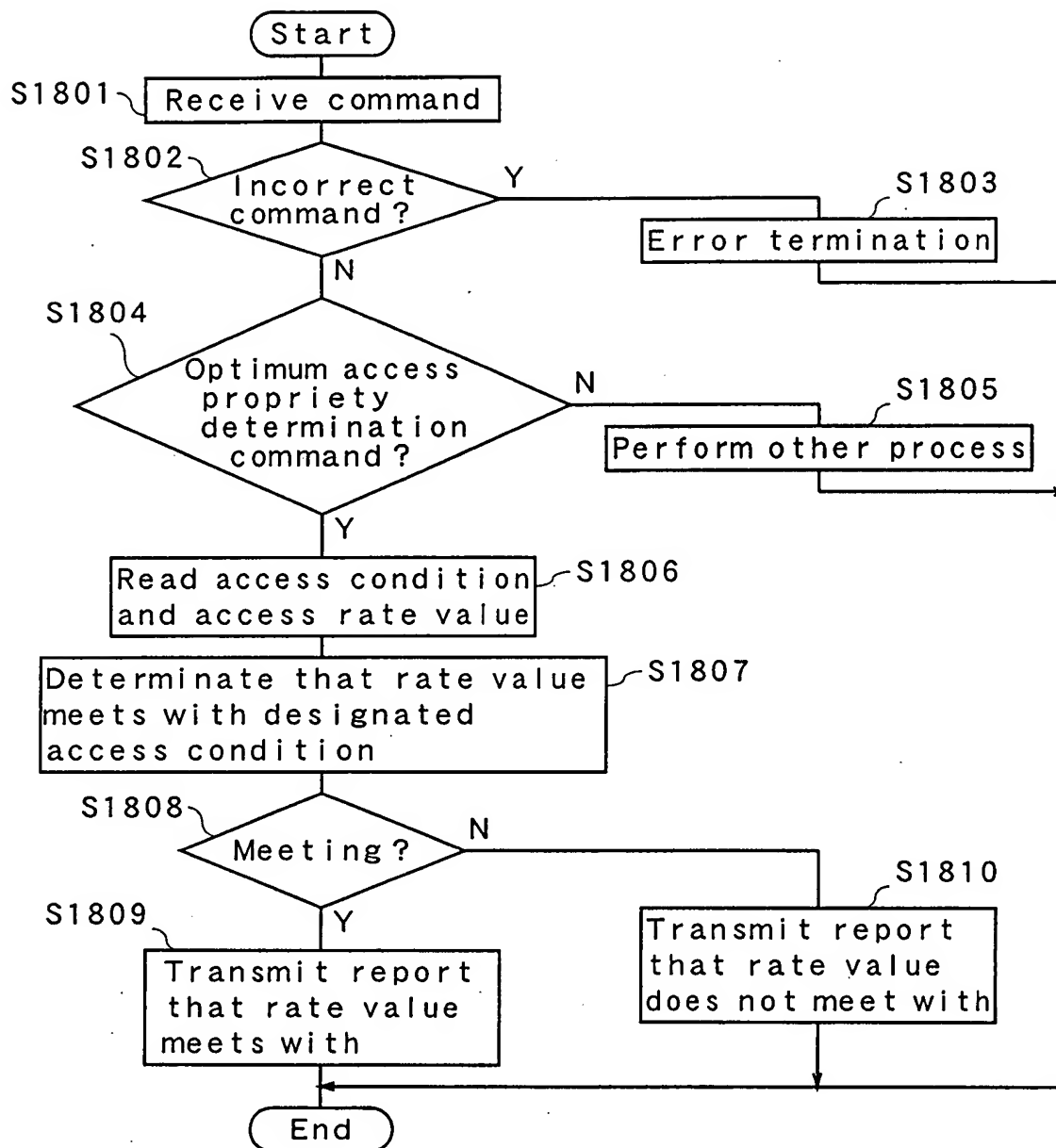


FIG. 19

(a)

		Process contents		
		Reading	Writing	Erasing
Rate performance level	High	Standard trans. rate $\geq 8.0 \text{ MB/s}$	Standard trans. rate $\geq 8.0 \text{ MB/s}$	Standard trans. rate $\geq 8.0 \text{ MB/s}$
	Medium	$4.0 \text{ MB/s} \leq \text{Standard trans. rate} \leq 8.0 \text{ MB/s}$	$4.0 \text{ MB/s} \leq \text{Standard trans. rate} \leq 8.0 \text{ MB/s}$	$4.0 \text{ MB/s} \leq \text{Standard trans. rate} \leq 8.0 \text{ MB/s}$
	Low	Standard trans. rate $< 4.0 \text{ MB/s}$	Standard trans. rate $< 4.0 \text{ MB/s}$	Standard trans. rate $< 4.0 \text{ MB/s}$

(b)

Transfer rate	Rate performance level
Transfer rate of reading(standard) = 11 MB/s	High
Transfer rate of writing(standard) = 10 MB/s	High
Transfer rate of erasing(standard) = 10.3 MB/s	High
Transfer rate of reading(worst) = 6 MB/s	High
Transfer rate of writing(worst) = 5 MB/s	High
Transfer rate of erasing(worst) = 5.1 MB/s	High

FIG. 20

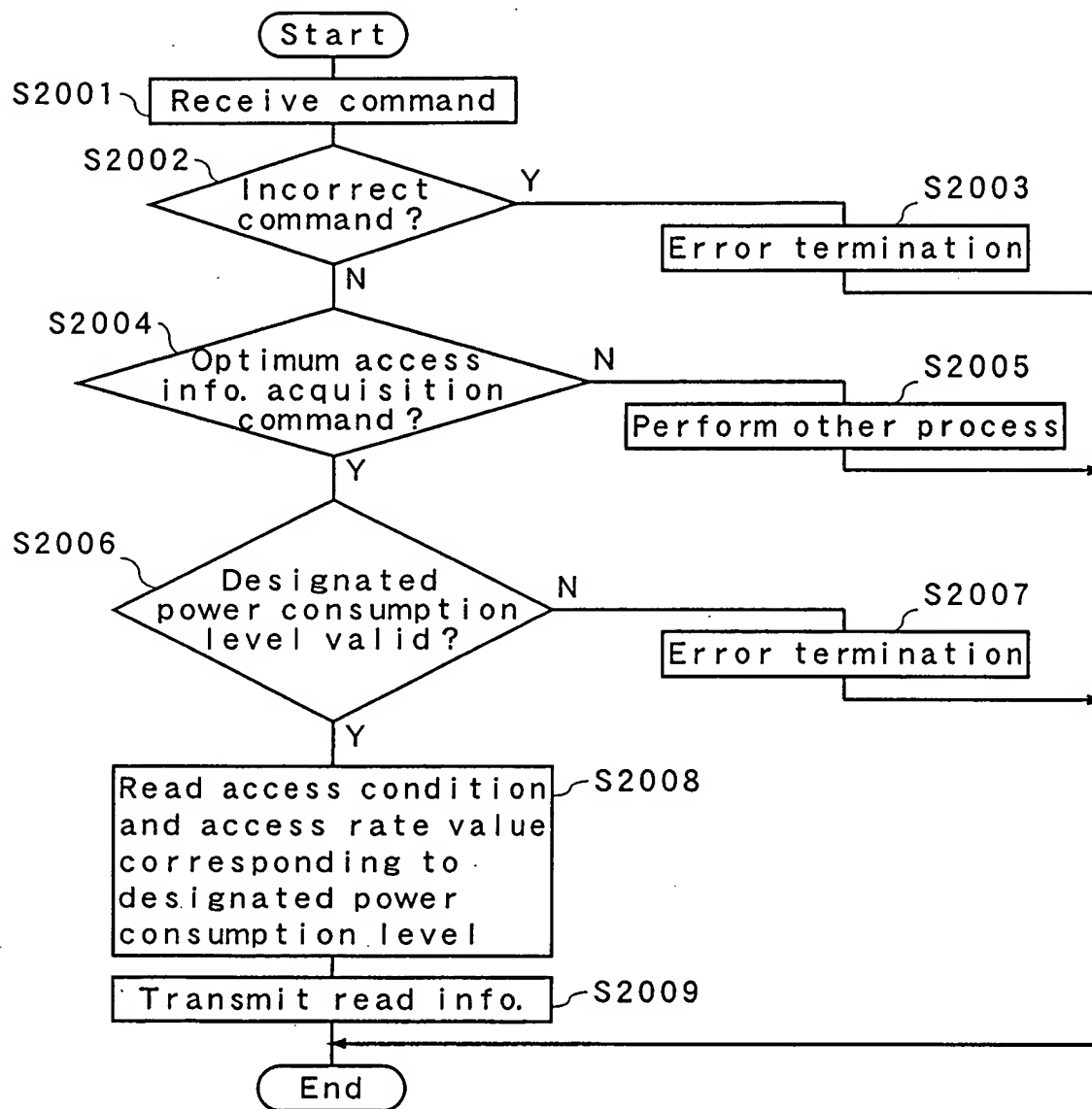


FIG. 21

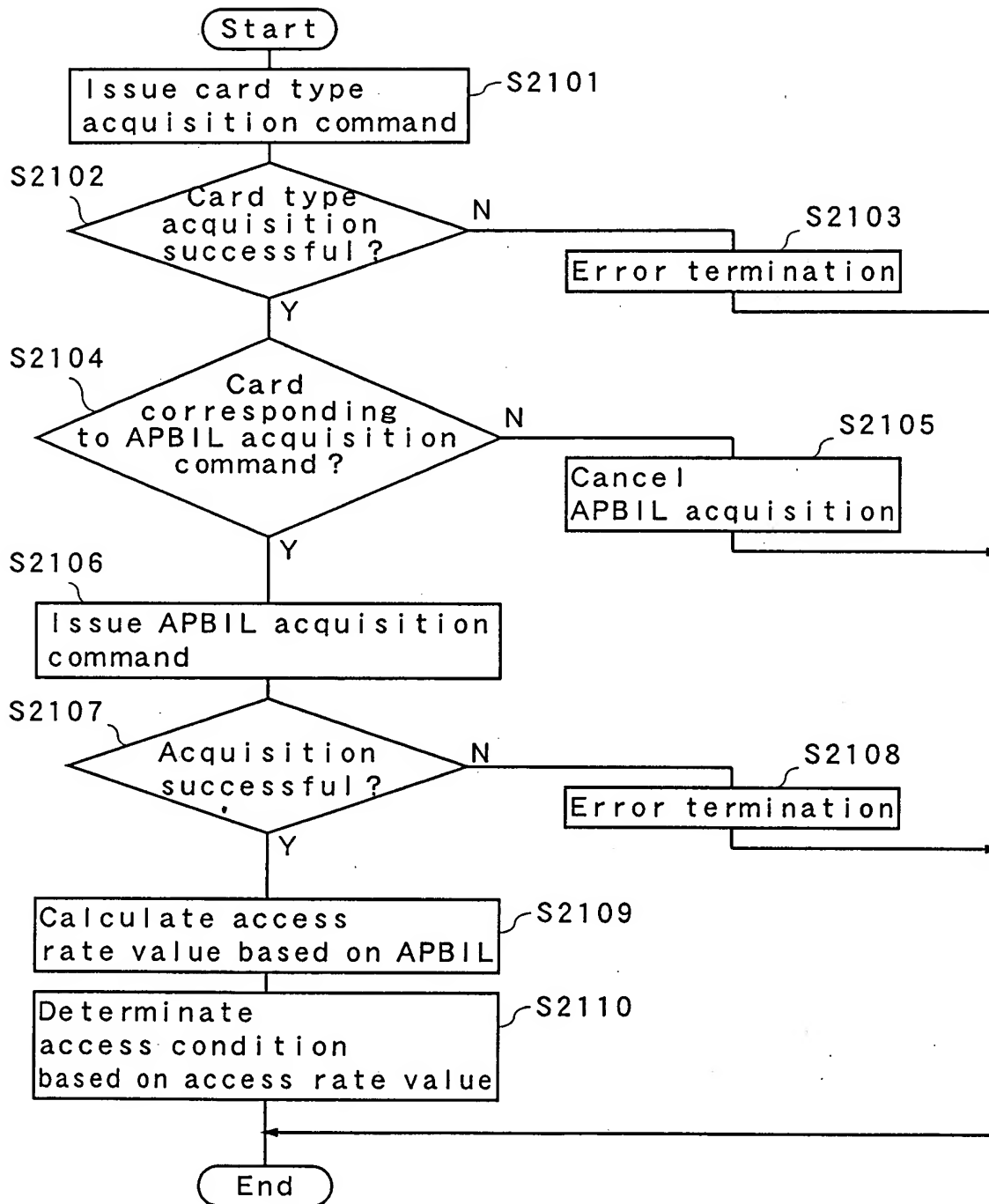


FIG. 22

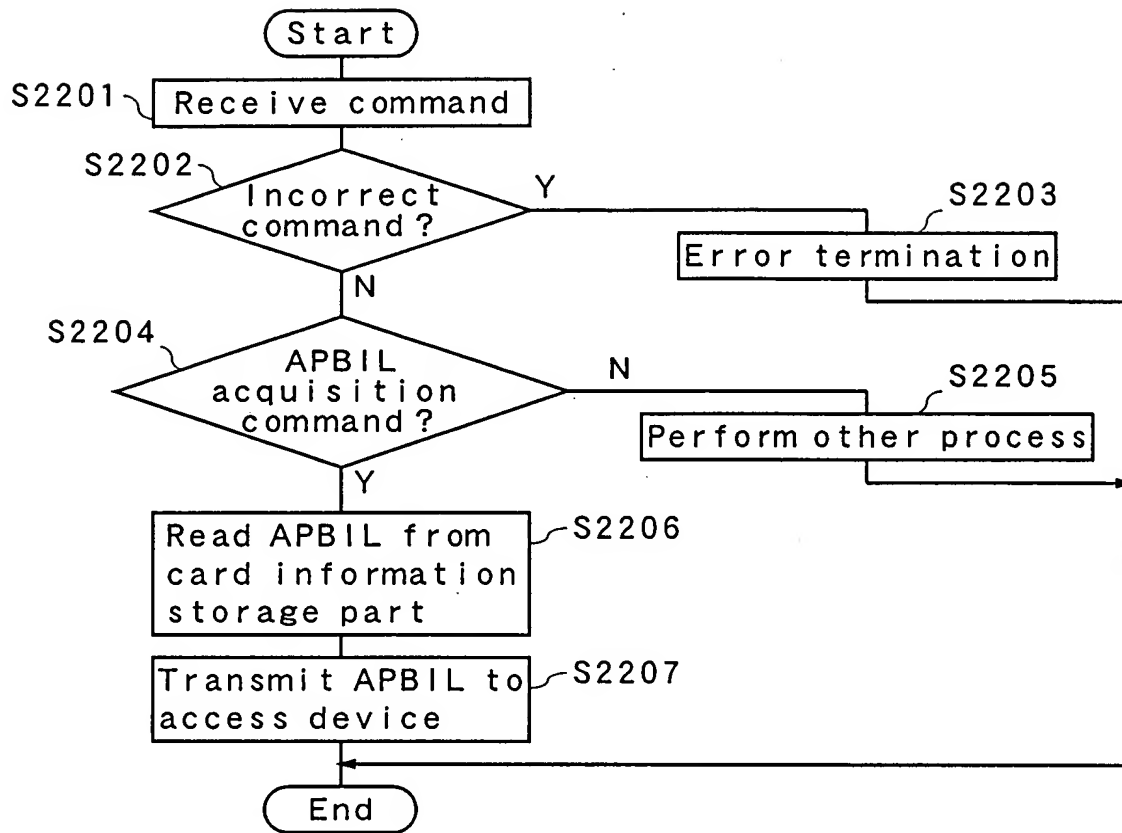


FIG. 23

(a)

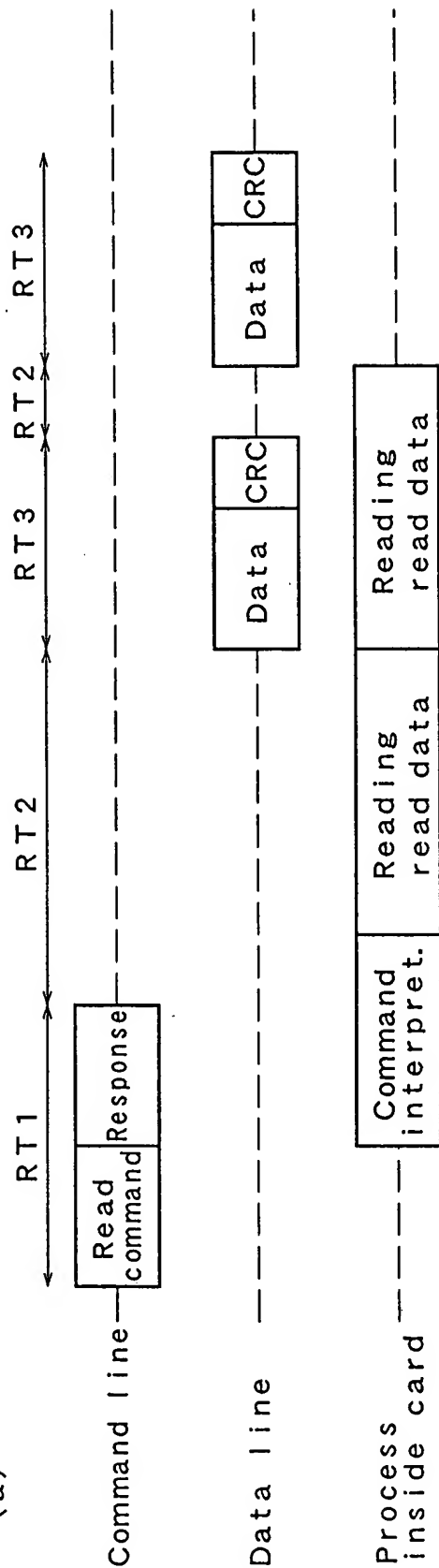
Process contents			APBIL
Reading	Writing	Erasing	
Table 1-A	Table 1-B	Table 1-C	

(b)

	Standard value		Worst value	
	SA	RA	SA	RA
Process unit size	512 Bytes	17 ms	25 ms	51 ms
	16 KB	43 μ s	690 μ s	1.6 ms
	128 KB	9.2 μ s	22 μ s	86 μ s
	256 KB	9.2 μ s	22 μ s	86 μ s
	1 MB	9.2 μ s	22 μ s	86 μ s

FIG. 24

(a)



(b)

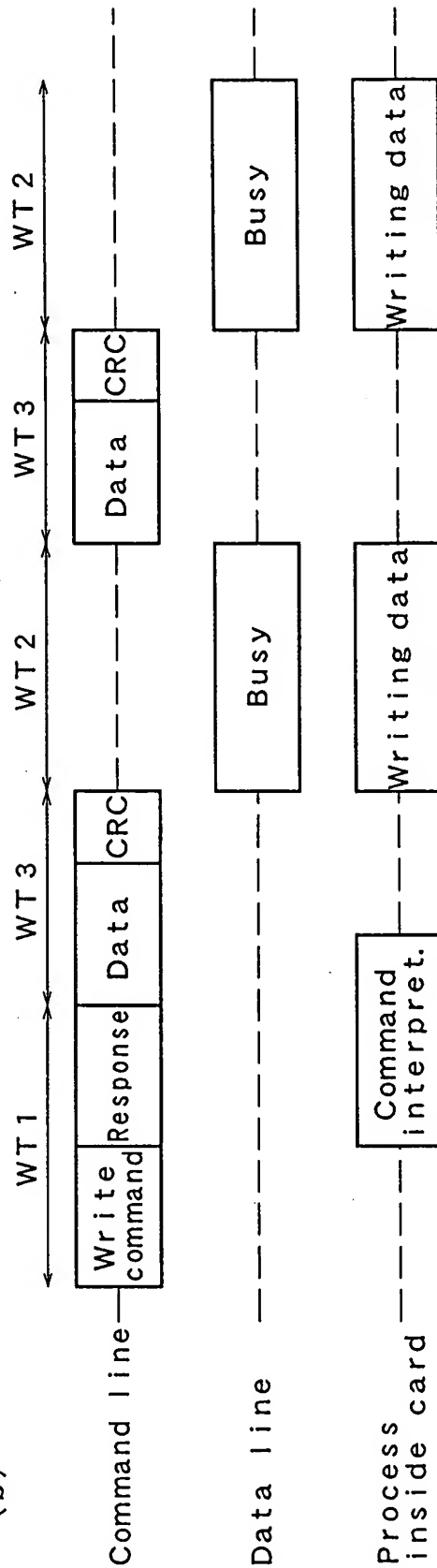


FIG. 25

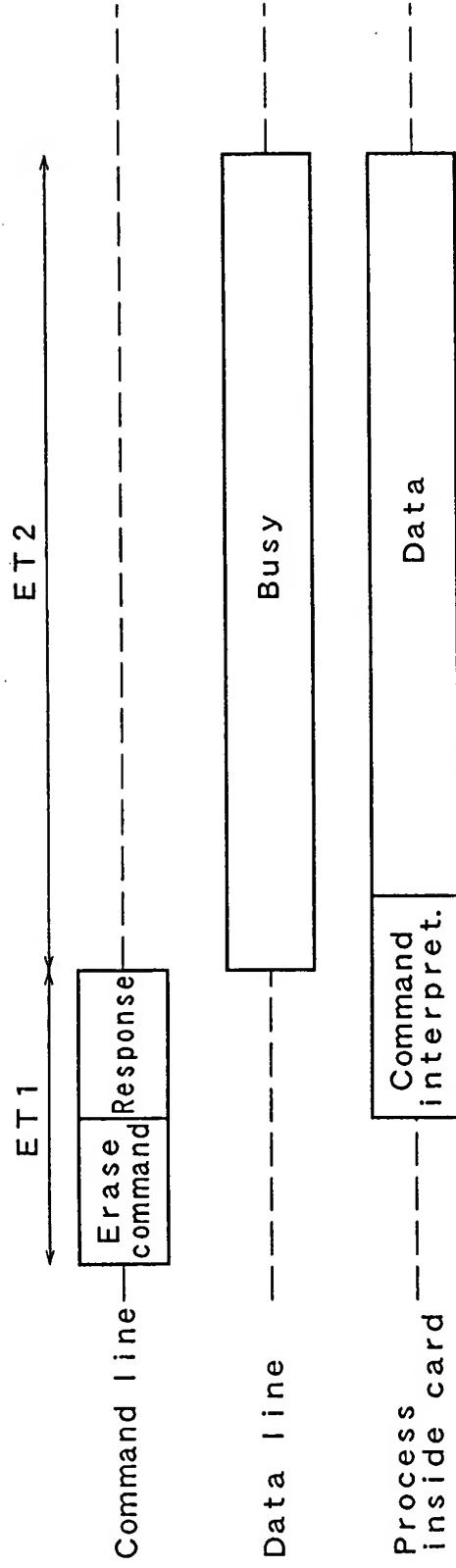


FIG. 26

(a)

		Process contents		
		Reading	Writing	Erasing
Input clock	12.5 MHz	Table 1-A	Table 1-B	Table 1-C
	25 MHz	Table 2-A	Table 2-B	Table 2-C
	50 MHz	Table 3-A	Table 3-B	Table 3-C

(b)

		Standard value		Worst value	
		SA	RA	SA	RA
Process unit size	512 Bytes	0.03 MB/s	0.02 MB/s	0.02 MB/s	0.01 MB/s
	16 KB	6 MB/s	0.7 MB/s	3 MB/s	0.3 MB/s
	128 KB	10 MB/s	8 MB/s	5 MB/s	4 MB/s
	256 KB	10 MB/s	8 MB/s	5 MB/s	4 MB/s
	1 MB	10 MB/s	8 MB/s	5 MB/s	4 MB/s

FIG. 27

(a)

	Process contents		
	Reading	Writing	Erasing
Input clock	12.5 MHz Table 1-A	Table 1-B	Table 1-C
	25 MHz Table 2-A	Table 2-B	Table 2-C
	50 MHz Table 3-A	Table 3-B	Table 3-C

(b)

	Standard value		Worst value	
	SA	RA	SA	RA
Process unit size	512 Bytes	17 ms	26 ms	51 ms
	16 KB	3 ms	23 ms	55 ms
	128 KB	13 ms	16 ms	33 ms
	256 KB	26 ms	33 ms	66 ms
	1 MB	105 ms	131 ms	262 ms

FIG. 28

(a)

	Process contents		
	Reading	Writing	Erasing
Input clock	12.5 MHz Table 1-A	Table 1-B	Table 1-C
	25 MHz Table 2-A	Table 2-B	Table 2-C
	50 MHz Table 3-A	Table 3-B	Table 3-C

(b)

	Standard value		Worst value	
	SA	RA	SA	RA
Process unit size	512 Bytes	0.03 MB/s	0.02 MB/s	0.01 MB/s
	16 KB	6 MB/s	3 MB/s	0.3 MB/s
	128 KB	10 MB/s	5 MB/s	4 MB/s
	256 KB	10 MB/s	5 MB/s	4 MB/s
	1 MB	10 MB/s	5 MB/s	4 MB/s

FIG. 29

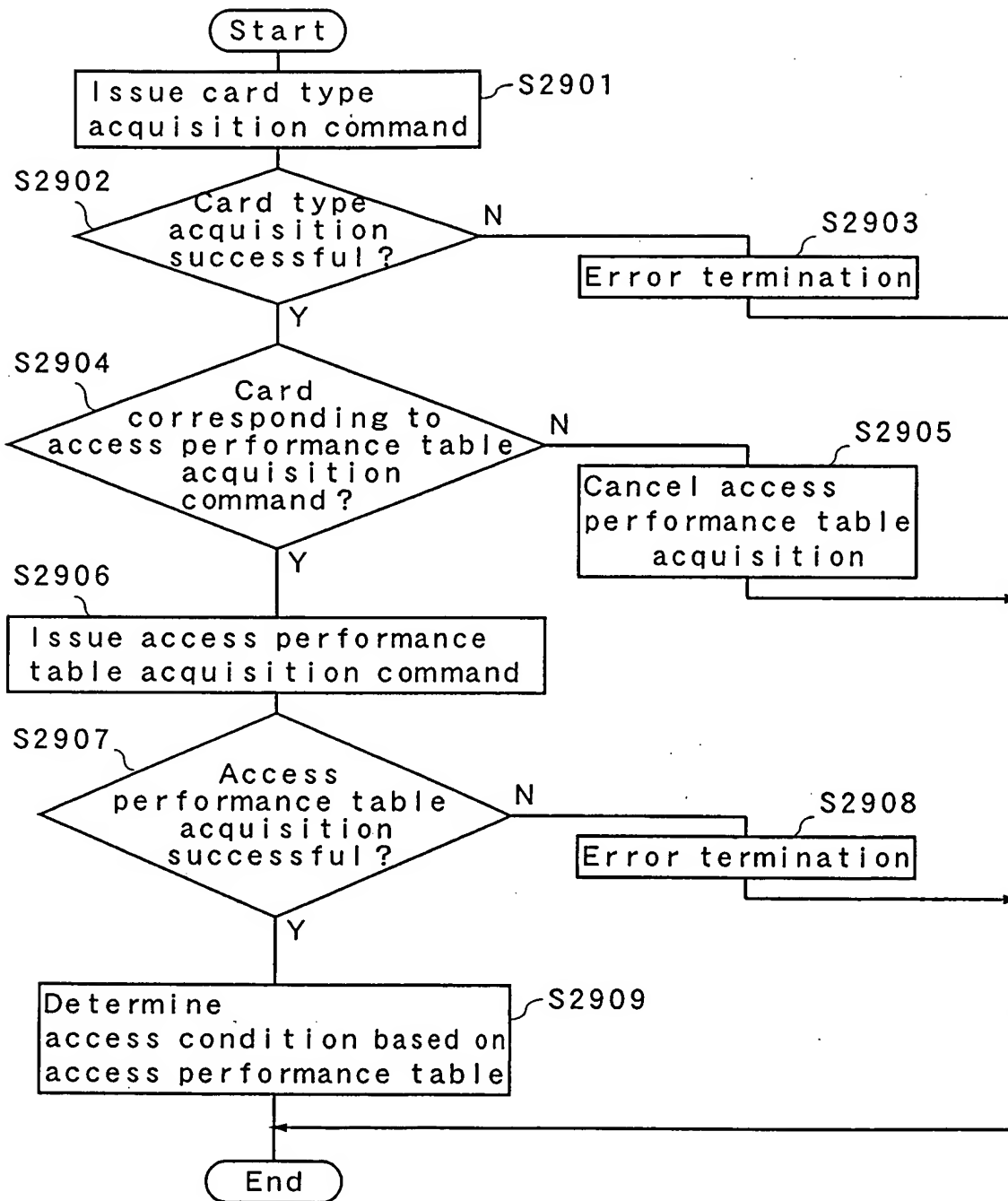


FIG. 30

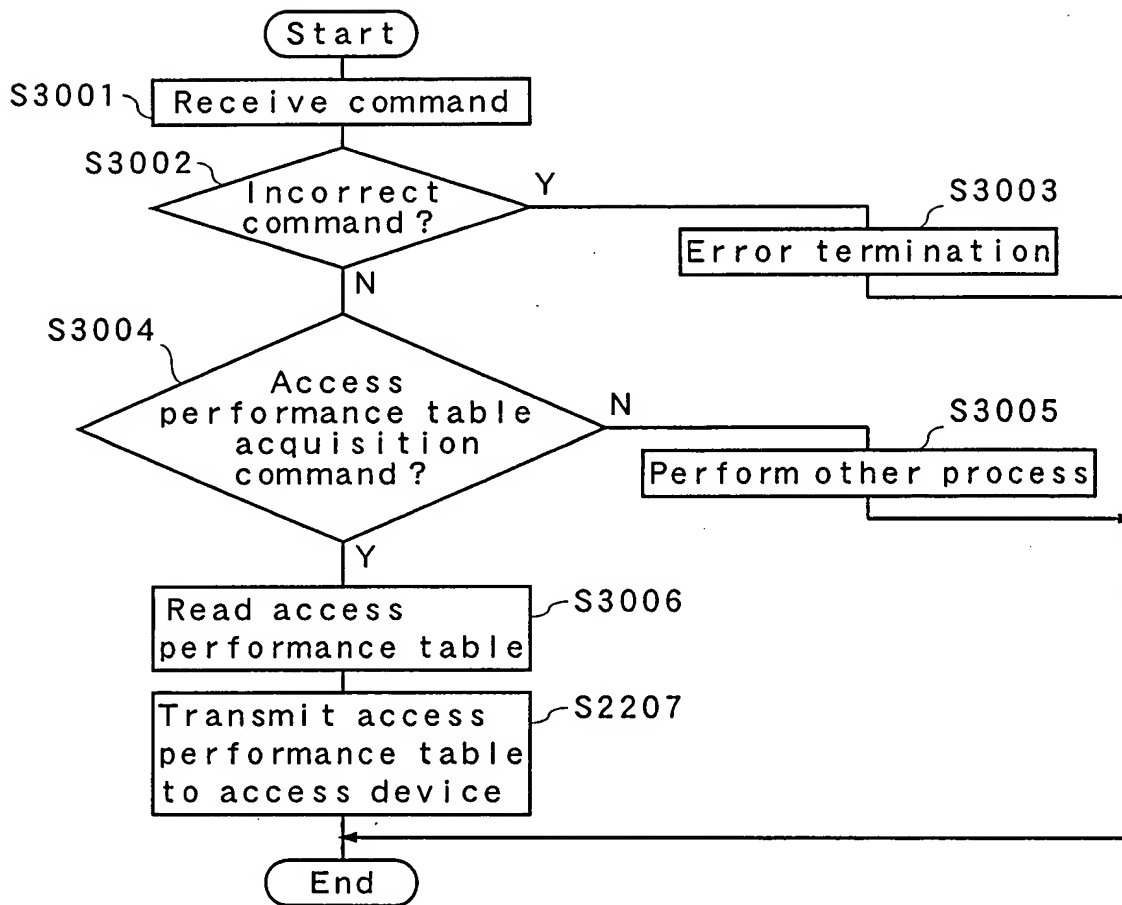


FIG. 31

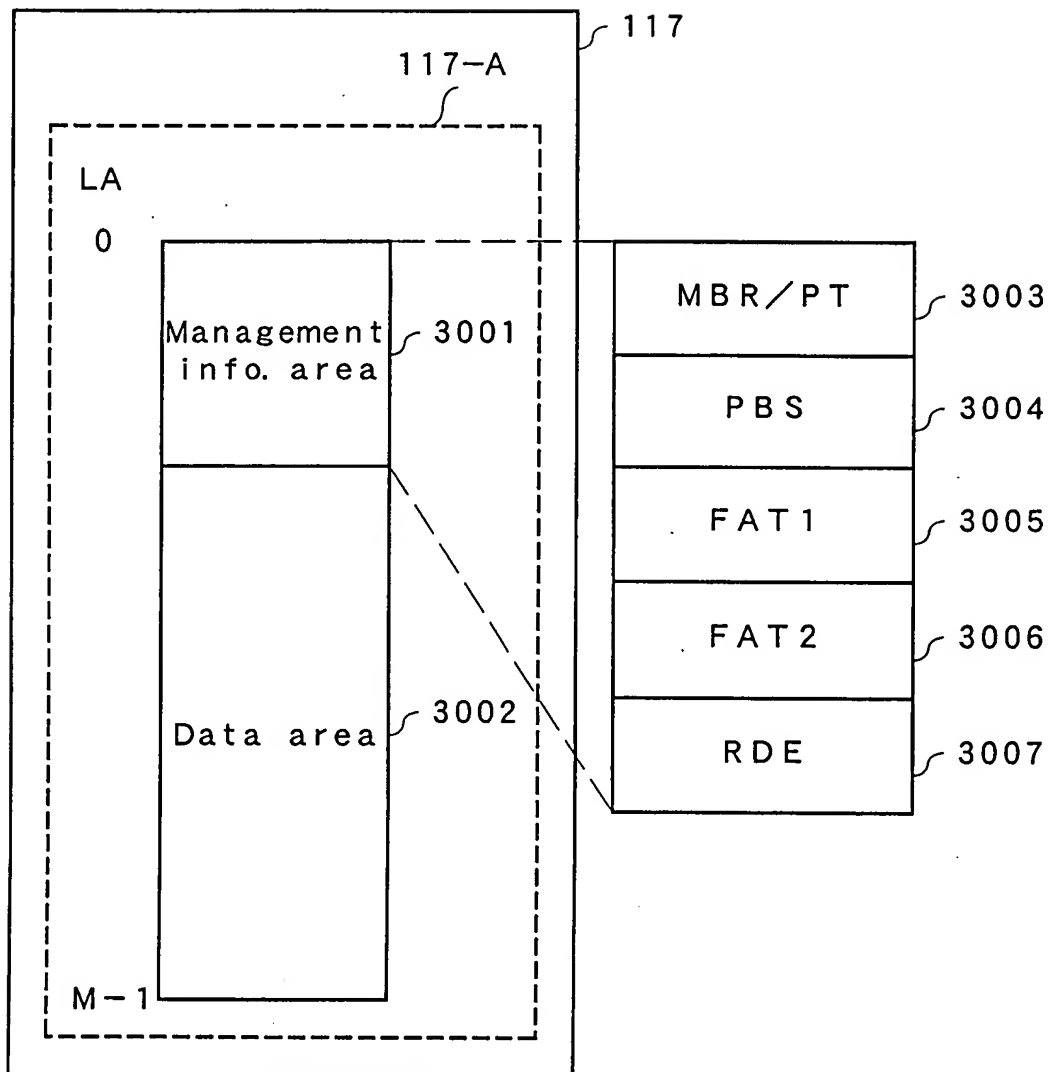


FIG. 32

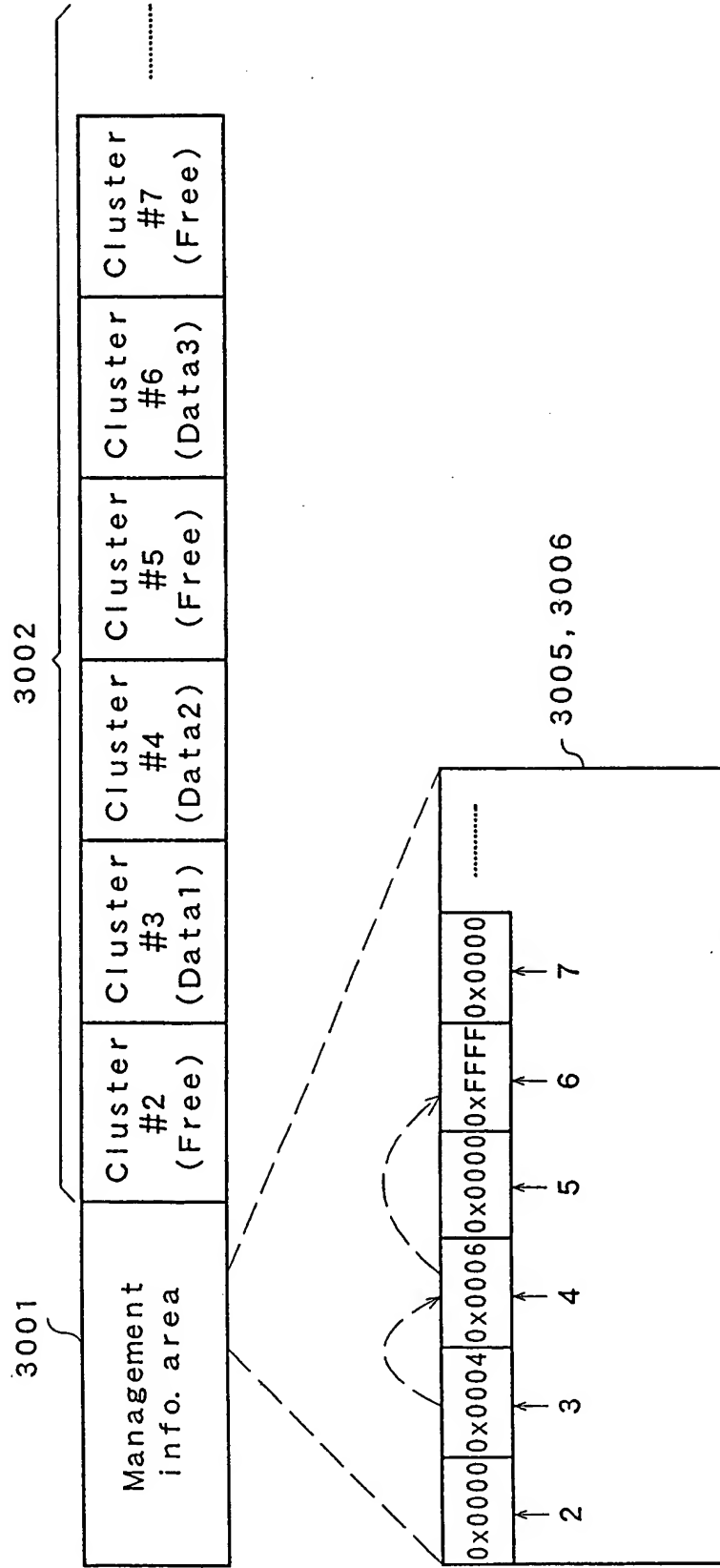


FIG. 33

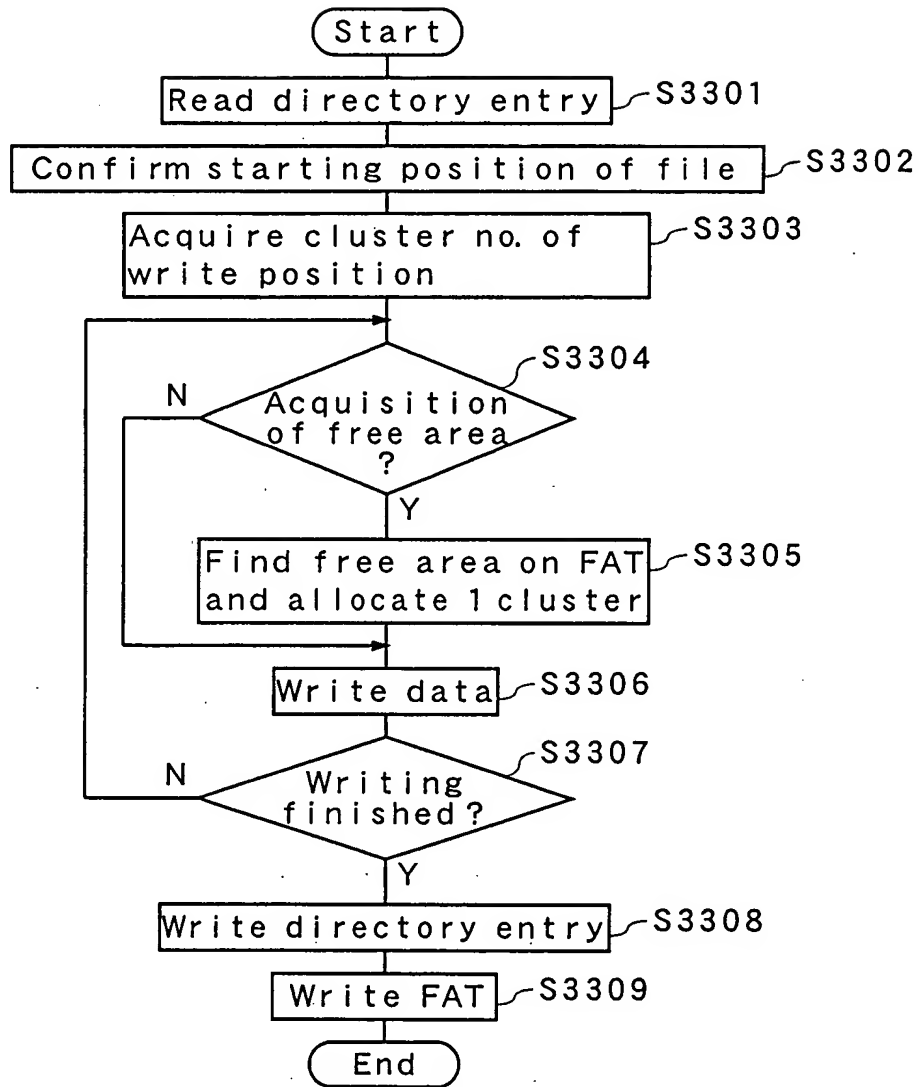
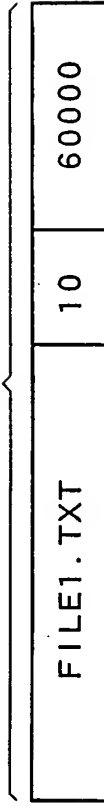


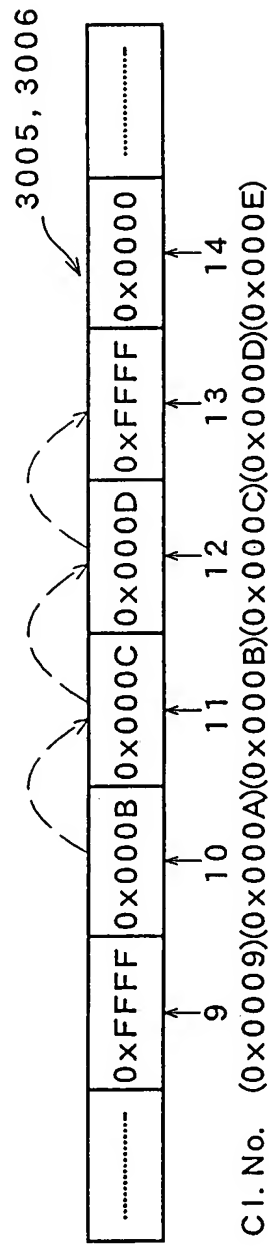
FIG. 34

3301

(a)



(b)



(c) CI.No.

3002

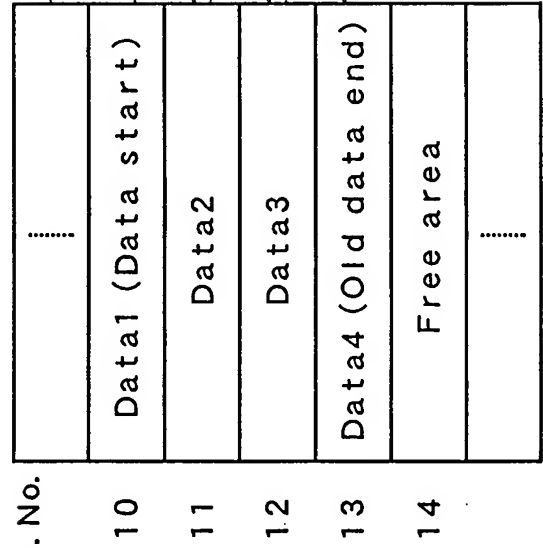
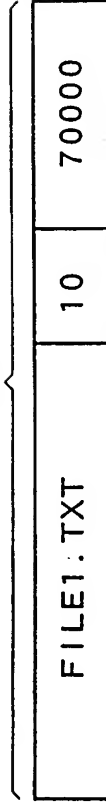


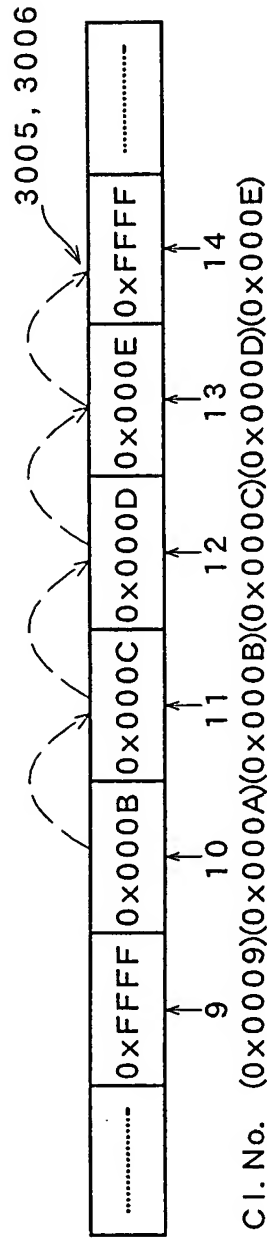
FIG. 35

3301

(a)



(b)



(c) CI. No.

3002

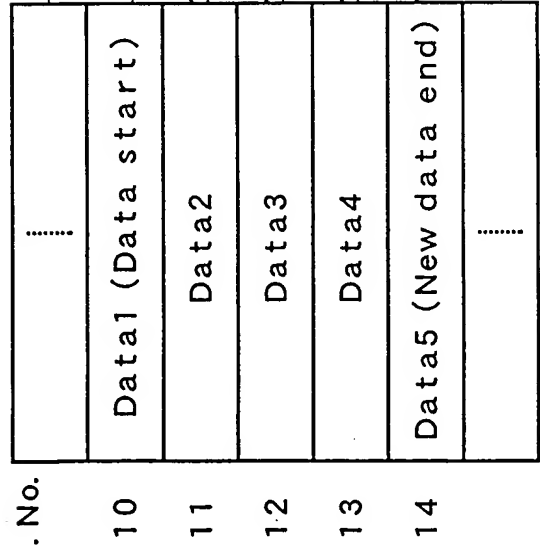


FIG. 36

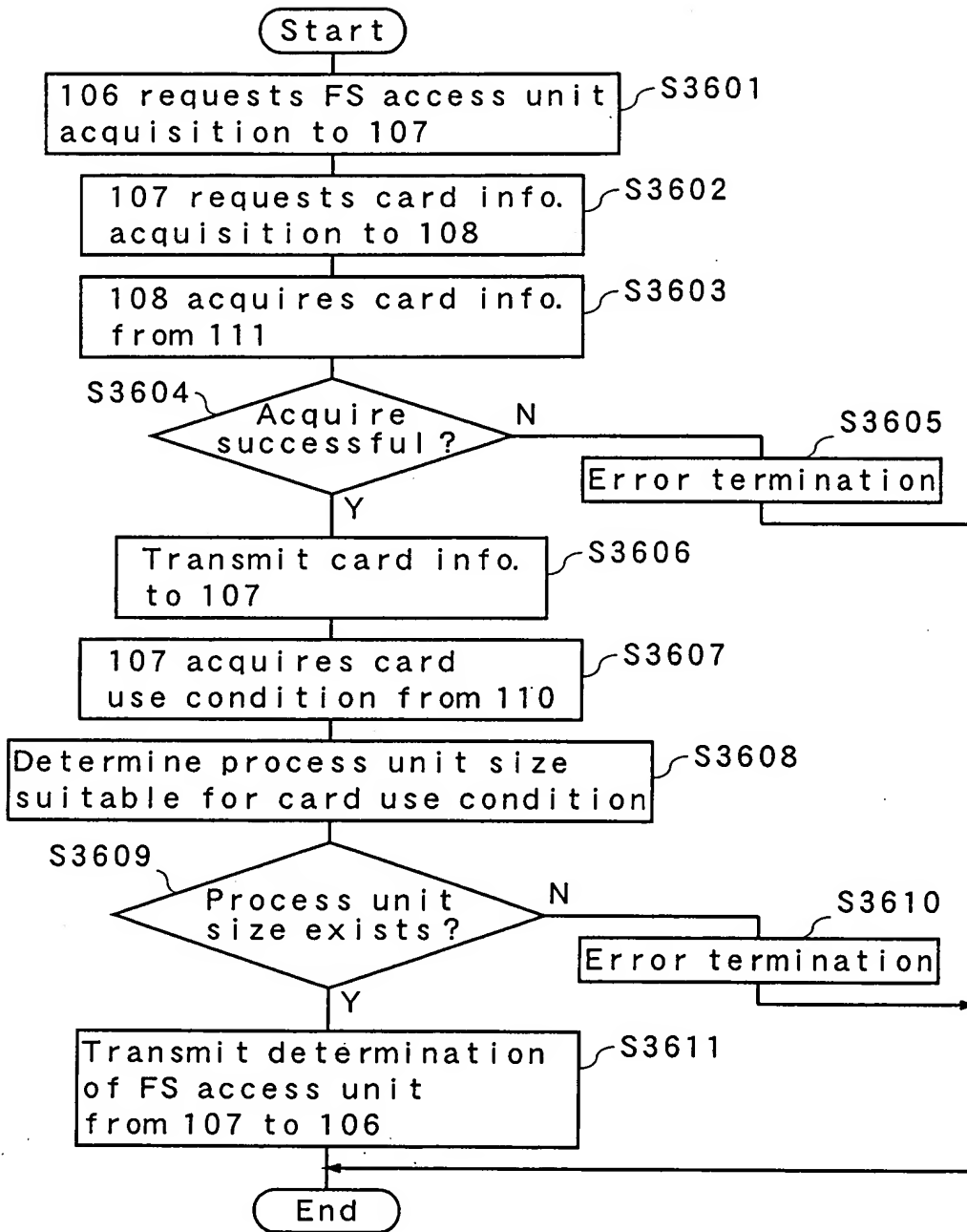


FIG. 37

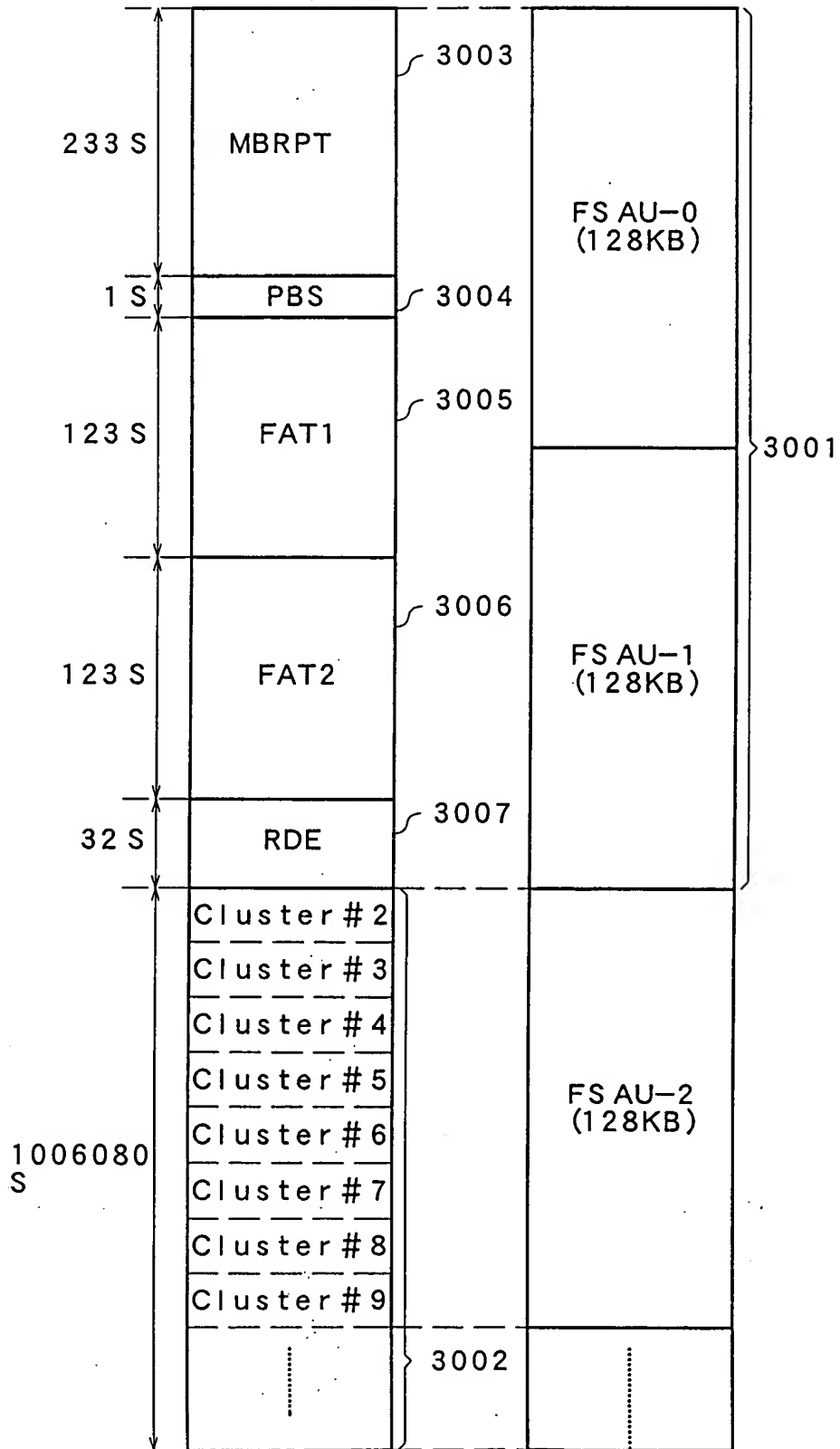


FIG. 38

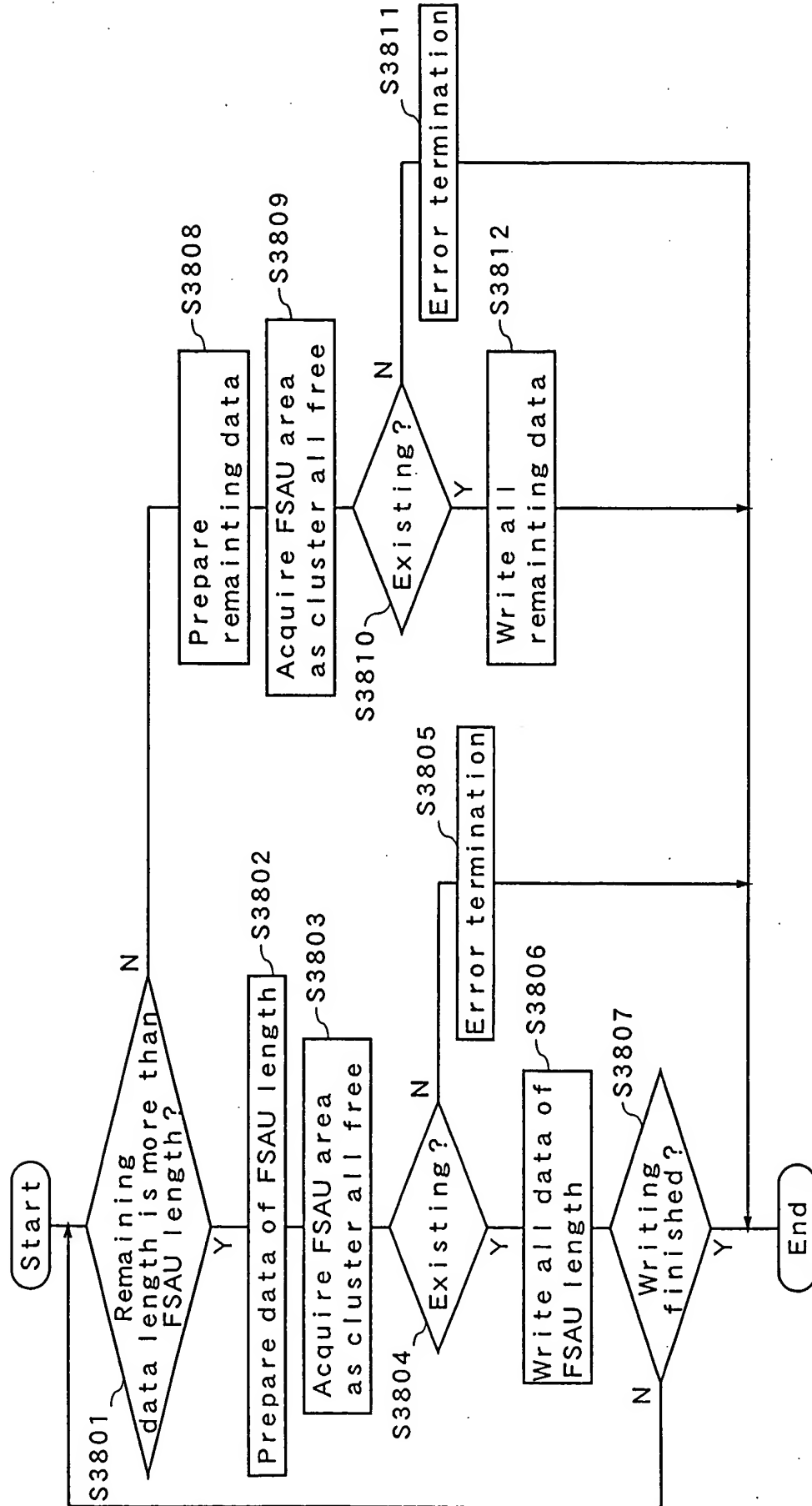


FIG. 39

3002

	CI. No.	
FSAU-0	2	FILE1
	3	FILE1
	4	Free
	5	Free
	6	Free
	7	Free
	8	Free
	9	Free
FSAU-1	10	DIR1
	11	DIR1
	12	Free
	13	Free
	14	Free
	15	Free
	16	Free
	17	Free
FSAU-2	18	Free
	19	Free
	20	Free
	21	Free
	22	Free
	23	Free
	24	Free
	25	Free

⋮

FIG. 40

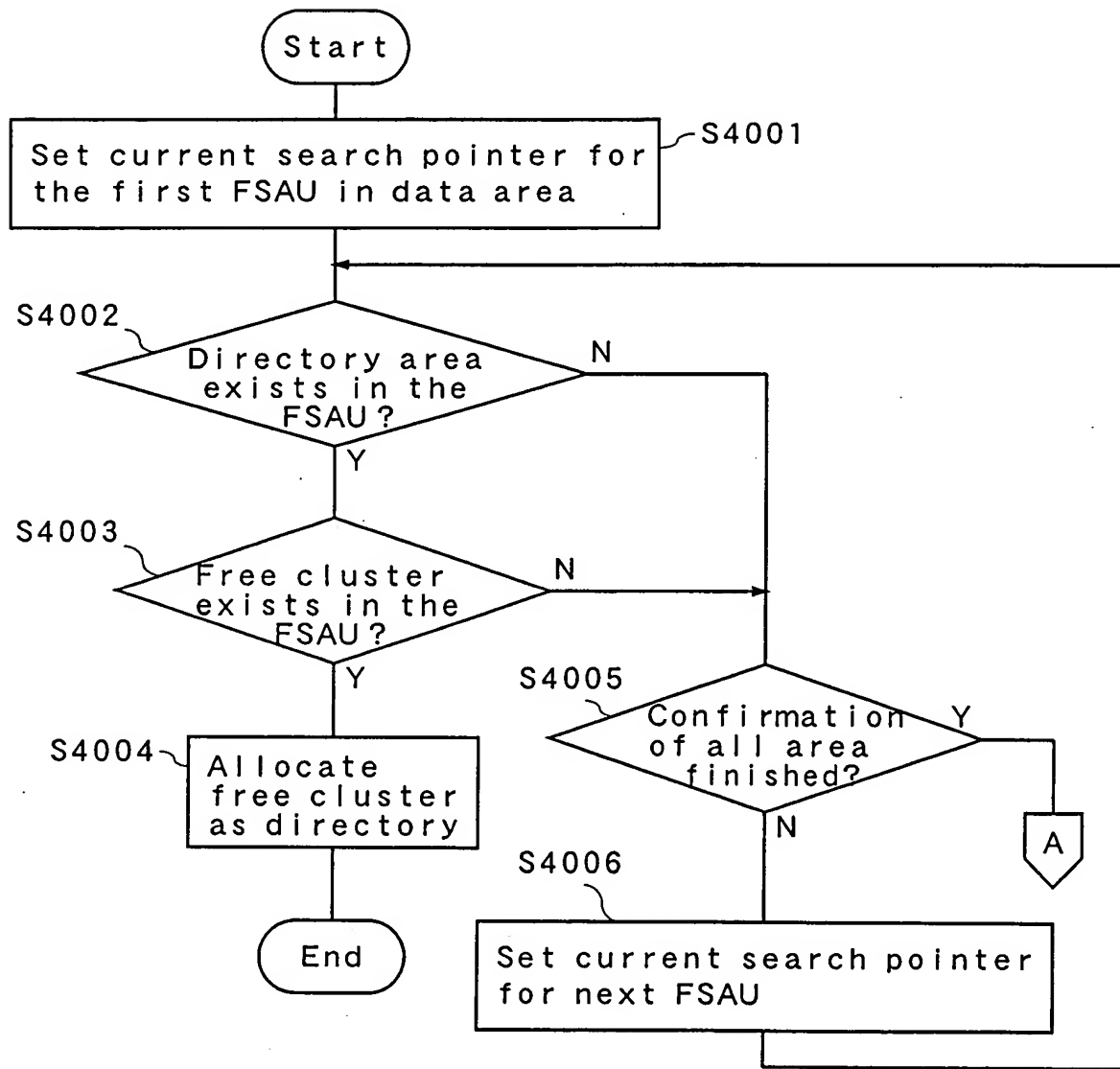


FIG. 41

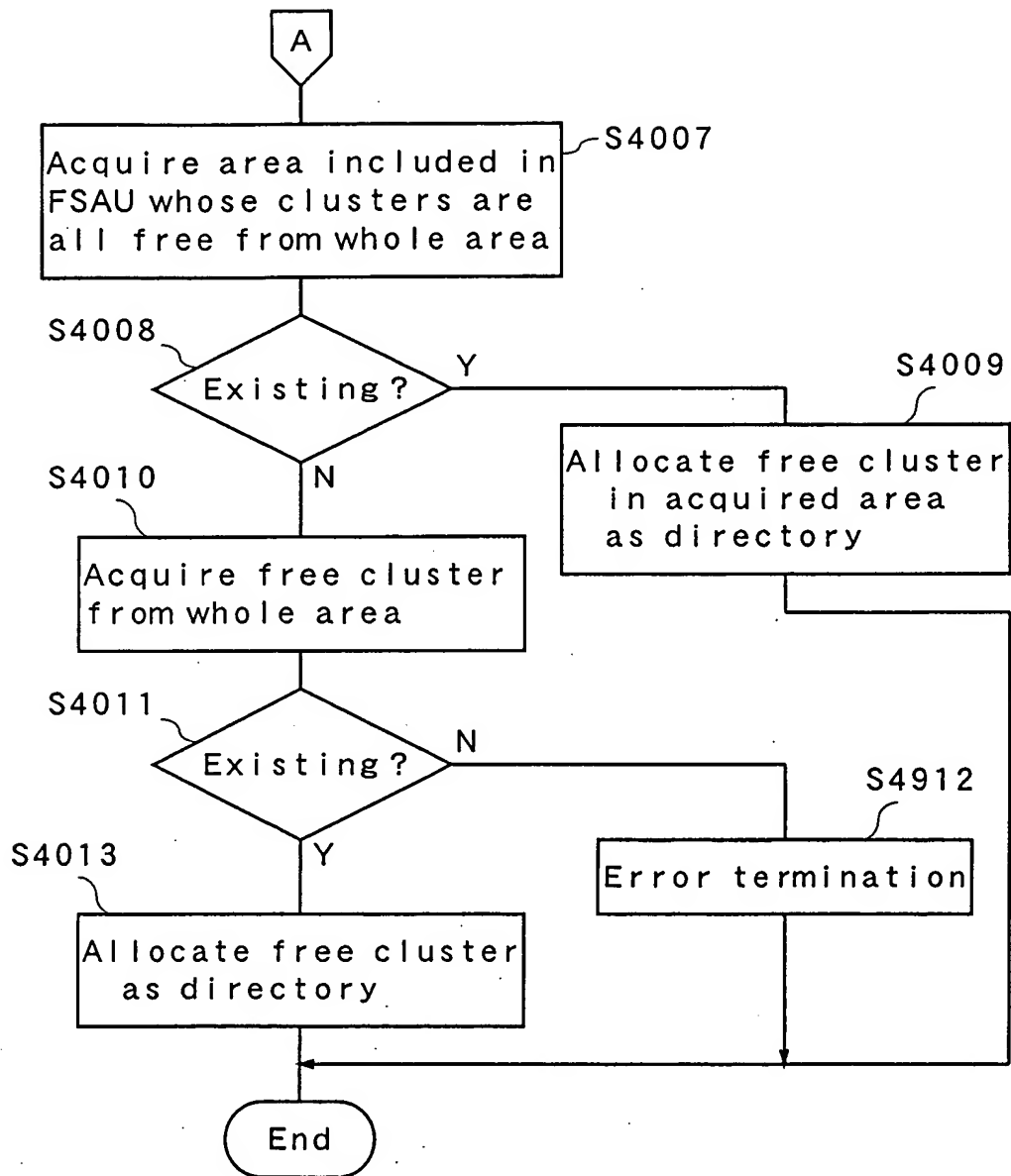


FIG. 42

CI. No.		3002
FSAU-0	2	FILE1
	3	FILE1
	4	Free
	5	Free
	6	Free
	7	Free
	8	Free
	9	Free
FSAU-1	10	DIR1
	11	DIR1
	12	Free
	13	Free
	14	Free
	15	Free
	16	Free
	17	Free
FSAU-2	18	Free
	19	Free
	20	Free
	21	Free
	22	Free
	23	Free
	24	Free
	25	Free

⋮

FIG. 43

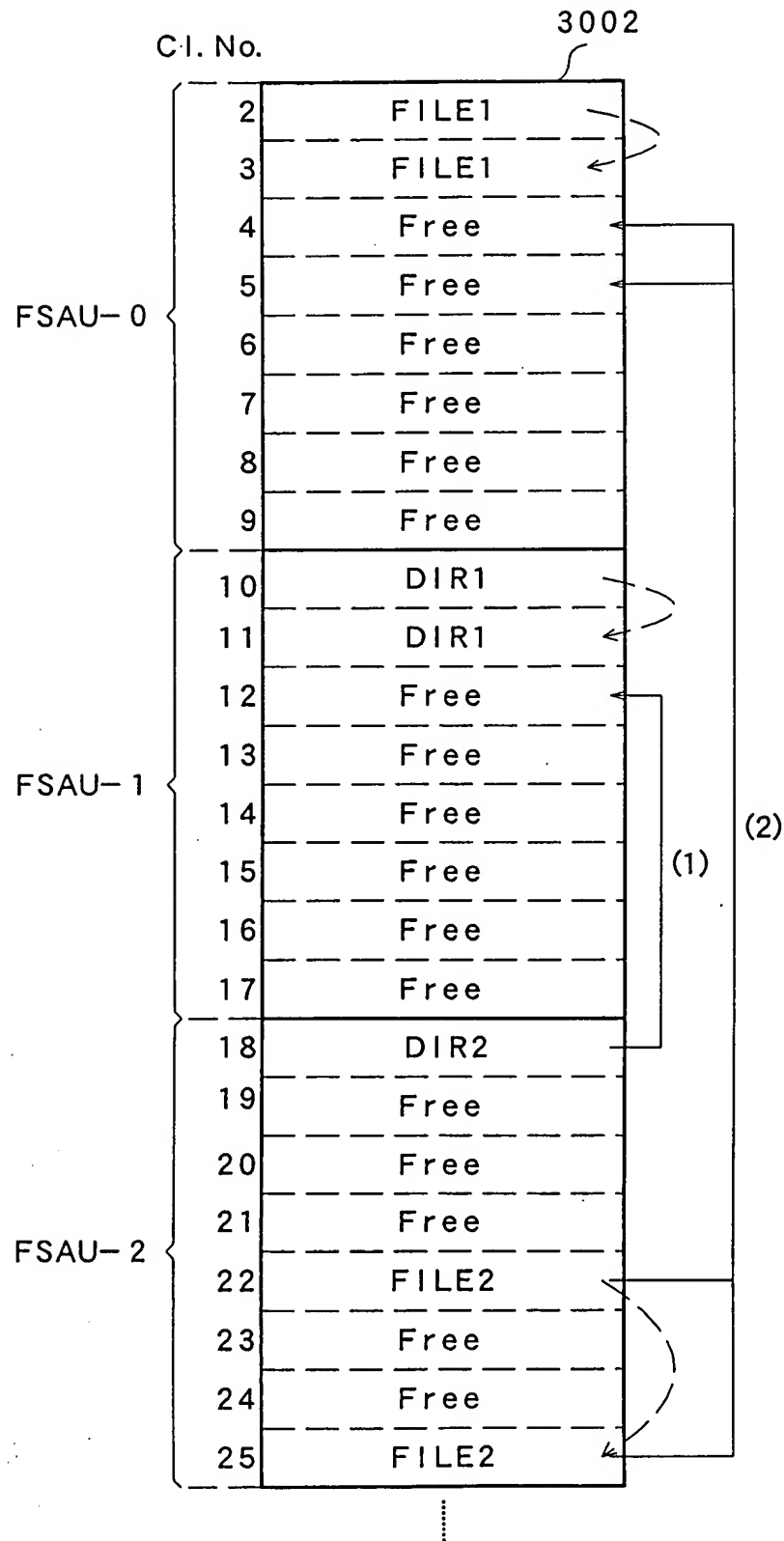


FIG. 44

CI. No.		3002
FSAU-0	2	FILE1
	3	FILE1
	4	FILE2
	5	FILE2
	6	Free
	7	Free
	8	Free
	9	Free
FSAU-1	10	DIR1
	11	DIR1
	12	DIR2
	13	Free
	14	Free
	15	Free
	16	Free
	17	Free
FSAU-2	18	Free
	19	Free
	20	Free
	21	Free
	22	Free
	23	Free
	24	Free
	25	Free

⋮

FIG. 45

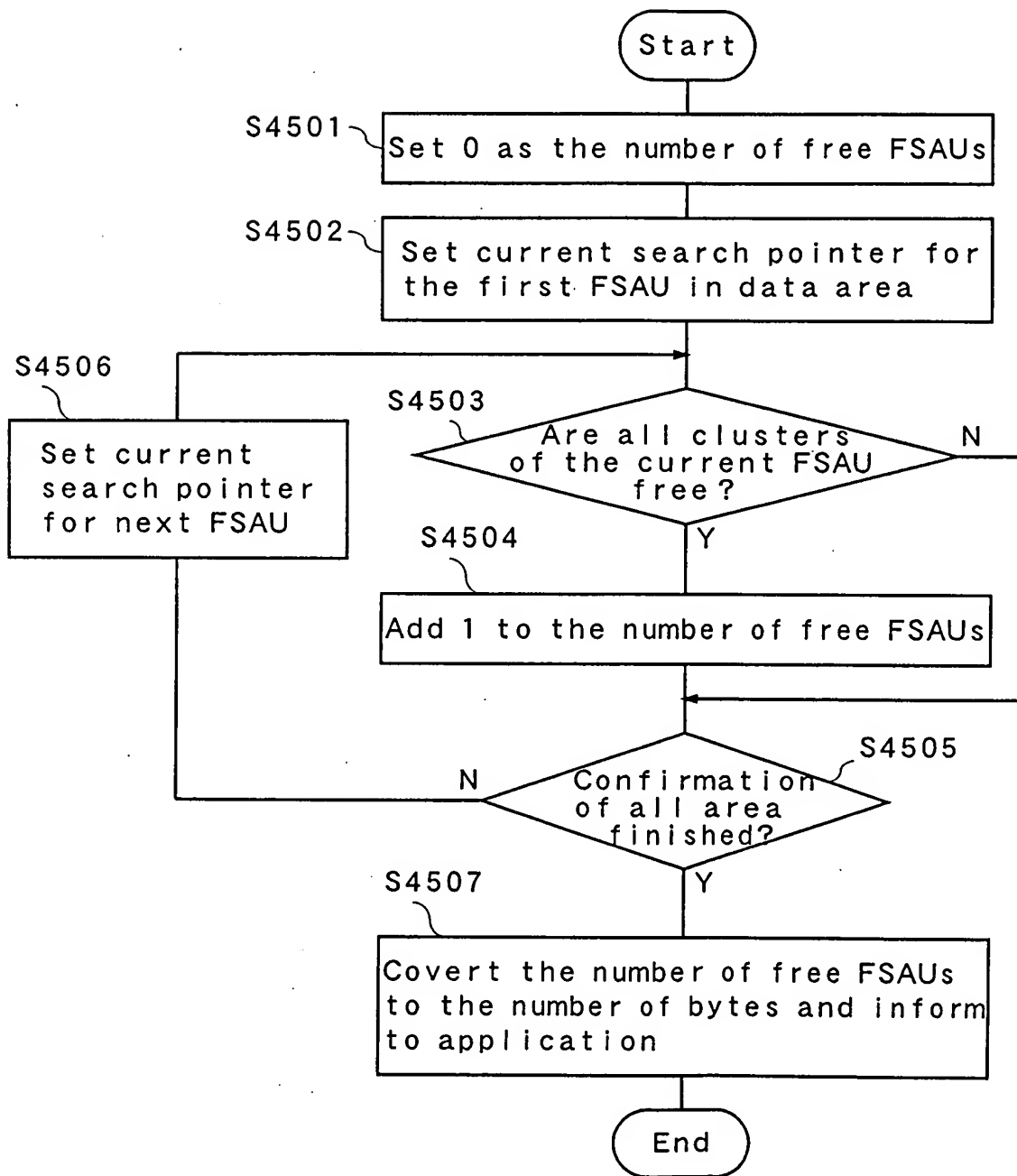


FIG. 46

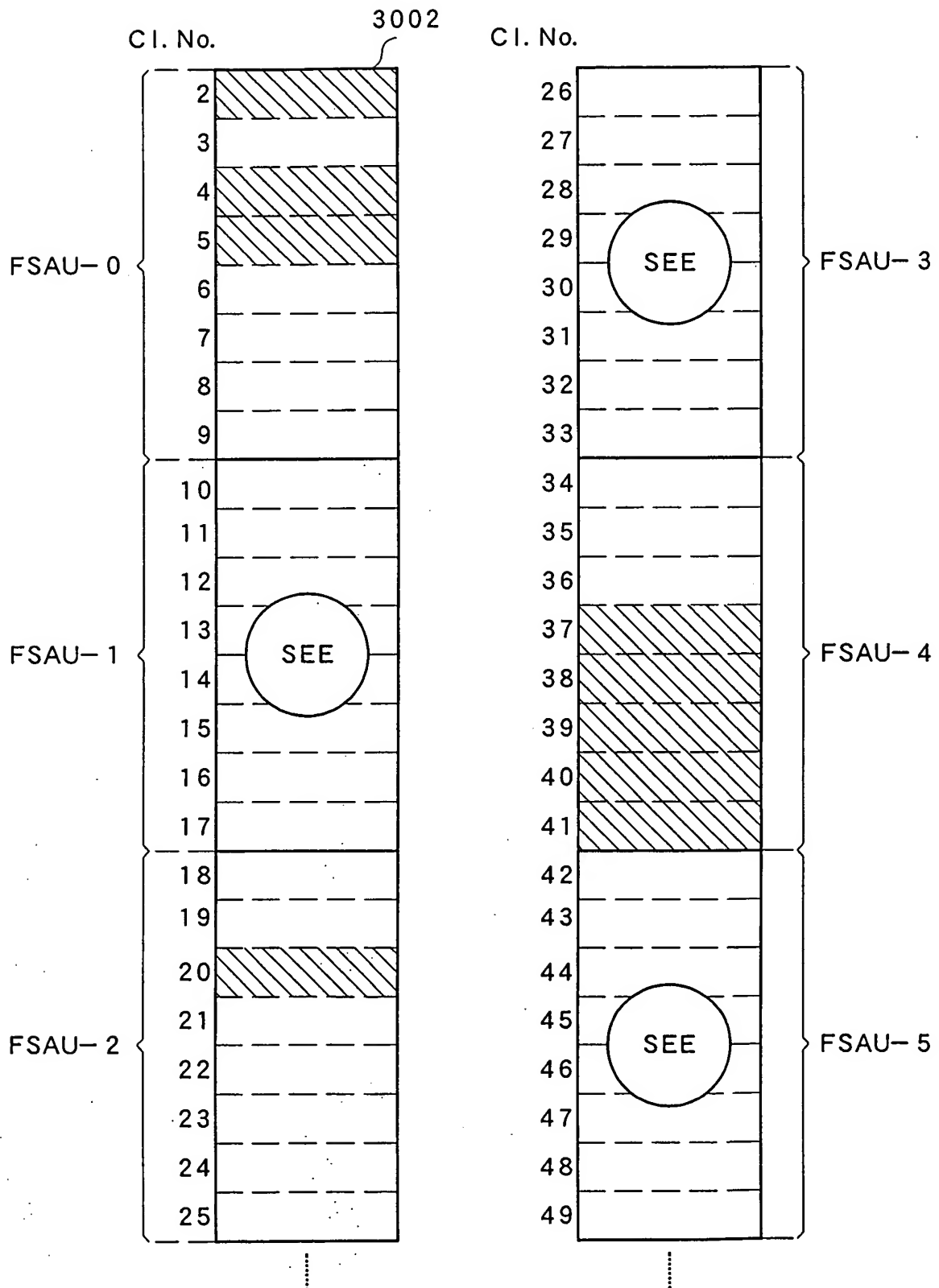


FIG. 47

